Name_____
Date_____
Section_____

Lab 3 Worksheet

Prelab

Part 1: Design a Binary Subtractor with 4-to-1 Multiplexers

1. Draw K-Maps for both outputs of the subtractor.

2. Draw the Logic Diagrams for both outputs of the subtractor using 4-to-1 MUXes.

3. Draw the Layout Diagram of the subtractor using 4-to-1 MUXes.

Part 1: Design a Binary Subtractor with 8-to-1 Multiplexers

1. Draw the Logic Diagrams for both outputs of the subtractor using 8-to-1 MUXes.

2. Draw the Layout Diagram of the subtractor using 8-to-1 MUXes.

Name_____
Date_____
Section_____

Postlab

Part 1: Design a Binary Subtractor with 4-to-1 Multiplexers

- ☐ Have TA verify that your breadboard circuit works. Signature_____
- ☐ Turn in a copy of your ***Lab3_1.vhd*** code. Do not turn in a copy of the test bench, just a copy of the file you changed.
- ☐ Turn in a copy of the simulation waveform.

Part 2: Design a Binary Subtractor with 8-to-1 Multiplexers

- ☐ Have TA verify that your breadboard circuit works. Signature_____
- ☐ Turn in copies of all of your VHDL code.
- ☐ Turn in a copy of the simulation waveform.