

Name _____
Date _____
Section _____

Lab 2 Worksheet

Part 1: Design a Binary Subtractor with 4-to-1 Multiplexers

Turn in copies of all of your VHDL code.

Turn in a copy of the simulation waveform.

Part 2: Design a Binary Subtractor with 8-to-1 Multiplexers

Turn in copies of all of your VHDL code.

Turn in a copy of the simulation waveform.