

ECE238

Homework Lab #1 (8 % Lab Grade) th

Due date : June 27 11:00 – 13:45 at Room 216

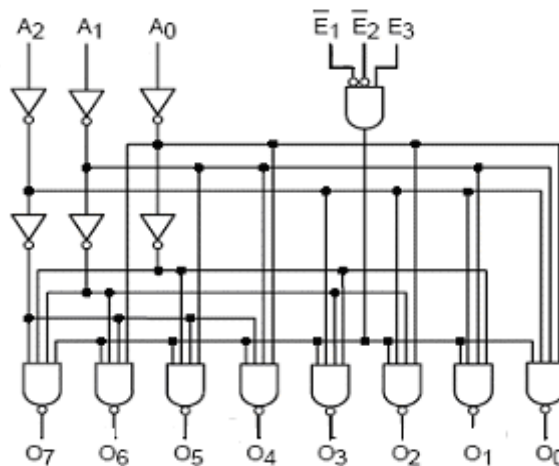
I highly recommend you to type every line of text so that you get a feel for the language's syntax. Use the syntax handouts and the lab reports as well. **Work on this assignment "ABSOLUTELY INDEPENDENTLY"**.

Please do not send your homework via email; turn in a printed version of your work.

Goal: Implement 1-8 decoder in VHDL

Introduction:

1-of-8 decoder accepts three binary weighted inputs (A_0 , A_1 , A_2) and when enabled provides eight mutually exclusive active LOW Outputs (O_0' – O_7'). The decoder features three Enable inputs, E_1' , E_2' , E_3 . All outputs will be HIGH unless E_1' and E_2' are LOW and E_3 is HIGH. The logic diagram and the truth table are shown in the following figures:



| INPUTS | | | | | | OUTPUTS | | | | | | | |
|-------------|-------------|-------|-------|-------|-------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| \bar{E}_1 | \bar{E}_2 | E_3 | A_0 | A_1 | A_2 | \bar{O}_0 | \bar{O}_1 | \bar{O}_2 | \bar{O}_3 | \bar{O}_4 | \bar{O}_5 | \bar{O}_6 | \bar{O}_7 |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| X | X | L | X | X | X | H | H | H | H | H | H | H | H |
| L | L | H | L | L | L | L | H | H | H | H | H | H | H |
| L | L | H | H | L | L | H | L | H | H | H | H | H | H |
| L | L | H | L | H | L | H | H | L | H | H | H | H | H |
| L | L | H | H | H | L | H | H | H | L | H | H | H | H |
| L | L | H | L | L | H | H | H | H | H | L | H | H | H |
| L | L | H | H | L | H | H | H | H | H | H | L | H | H |
| L | L | H | L | H | H | H | H | H | H | H | H | L | H |
| L | L | H | H | H | H | H | H | H | H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Part A

Write a VHDL description for the decoder *by using just the logic diagram*. Use only concurrent signal assignment (**do not use processes!**). For references about concurrent signal assignment and signals, see the Power Point slides of Lab1.

The inputs and the outputs must all be *std_logic or bits*. Write a testbench for testing the design. A good testbench must check for all possible values that the design can get (use the truth table). Turn in the following:

1. Hardcopy of the VHDL code for your design and the testbench.
2. Hardcopy of the waveforms.

Part B

Write a VHDL description for the decoder by using the truth table. **Use processes instead of concurrent signal assignment**. For reference about processes, see Power Point slides of Lab 2.

I recommend you to use **if-then-else** statement for the enable signal and **case statement** to identify the active output. Revisit Power Point slides of Lab 2.

A0,A1,A2 must be *std_logic_vector*. Write a testbench for testing the design. Test your design for all possible input values. Turn in the following:

1. Hardcopy of the VHDL code for your design and the testbench.
2. Hardcopy of the waveforms