

ECE238
VHDL Homework #3 (7% Lab Grade)
Due date: July 20th 11:00-13:00 at Room 216

Sequential Logic

Write a VHDL description for a mod-99 counter that goes in step of R, where R is a 4-bit input in the range [0, 9]. The counter has two 4-bit outputs: MSD and LSD. The counter has also a 1-bit input RESET and a CLOCK input.

Here is an example of the behavior of the counter. Assume that R= "0100"; then the counter must count 0 (with outputs MSD = "0000", LSD = "0000"), 4 (MSD = "0000", LSD = "0100"), 8 (MSD = "0000", LSD = "1000"), 12 (MSD = "0001", LSD = "0010"), and so on. The counter must count up on every rising edge clock transition and must use *std_logic* datatype. Arithmetic operations on *std_logic* datatype are not part of VHDL standard but are provided by the package *std_logic_arith*.

In order to use the arithmetic operators defined in that package, you must add the following line before your entity declaration.

use IEEE.std_logic_arith.all;

Addition is achieved using the "+" operator. Some examples:

```
address_out <= address_in + offset;      -- adding two signals of same width
a <= b + "0101";                          -- signals a and b are 4-bit vectors
```

For this project, you have to simulate and turn in the source code and the result waveforms for two cases. The first one must show the outputs when the input R= "0011", while the second one must show the outputs when R = "1001".