Name_____
Date_____
Section_____

Lab Worksheet

Design Analisis

Draw a block diagram of what would be an 8-bit wide ripple carry adder.

Creating, synthetizing and simulating a Half Adder (HA) Step 1

- ☐ Turn in a copy of your completed ***half_adder.vhd*** code.

Creating, synthetizing and simulating a Full Adder (FA) Step 2

- ☐ Turn in a copy of your completed ***full_adder.vhd*** code.

Creating, synthetizing and simulating a 4-bit Full Adder (FA) Step 3

- ☐ Turn in a copy of your completed ***four_bit_full_adder_tb.vhd*** file.

Creating, synthetizing and simulating an Accumulator Step 4

- ☐ Turn in a copy of your completed ***accumulator.vhd*** code.

Implementing the Accumulator Step 5

☐ Have your TA verify that your accumulator works. Signature_____

Resources Analysis Step 6

How many CLBs is using your system?

Final Task Step 7

Demonstrate the system to the T.A
T.A signature:

Bonus Activity Step 8

Demonstrate the system to the T.A
T.A signature:

1. How many CLBs is using your system? Is it more or less than the original design? Why?
2. Print down your code for the accumulator and attach it to your final report.