ECE 238 Exam 2

Problem 1 20 /20

Problem 2 25 /25

Problem 3 30 /30

Problem 4 25 /25

Total 100

Name: Solutions

Good Luck!

1-1 / 2

Problem 1 (20 points total)

We would like to build a **Moore** circuit that outputs the sequence:

1, 0, 0, 0, 1, and the sequence repeats.

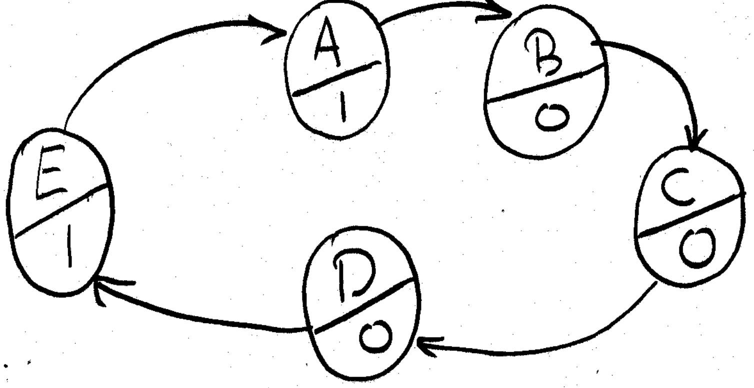
1(a)(4 points) Give the state diagram that realizes this sequence. *Hint:* You will need 5 states.

1(b)(8 points) Derive the state table for implementing the circuit using D flip-flops.

1(c)(5 points) Use K-maps to compute optimal expressions for the inputs to the D flip-flops.

1(d)(3 points) Show the final circuit.

1(a)



1(b)

Present State $Q_2Q_1Q_0$	Next State $D_2D_1D_0$ inputs,	Output
A: 000	B: 001	1
B: 001	C: 011	0
C: 011	D: 110	0
D: 110	E: 010	0
E: 010	A: 000	1

For the rest of the states: 111, 100, 101, next states and output are set to X.

1(c)

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	1	0
1	X	X	X	0

$D_2^+ = Q_1 Q_0$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	1	0
1	X	X	X	1

$D_1^+ = Q_2 + Q_0$

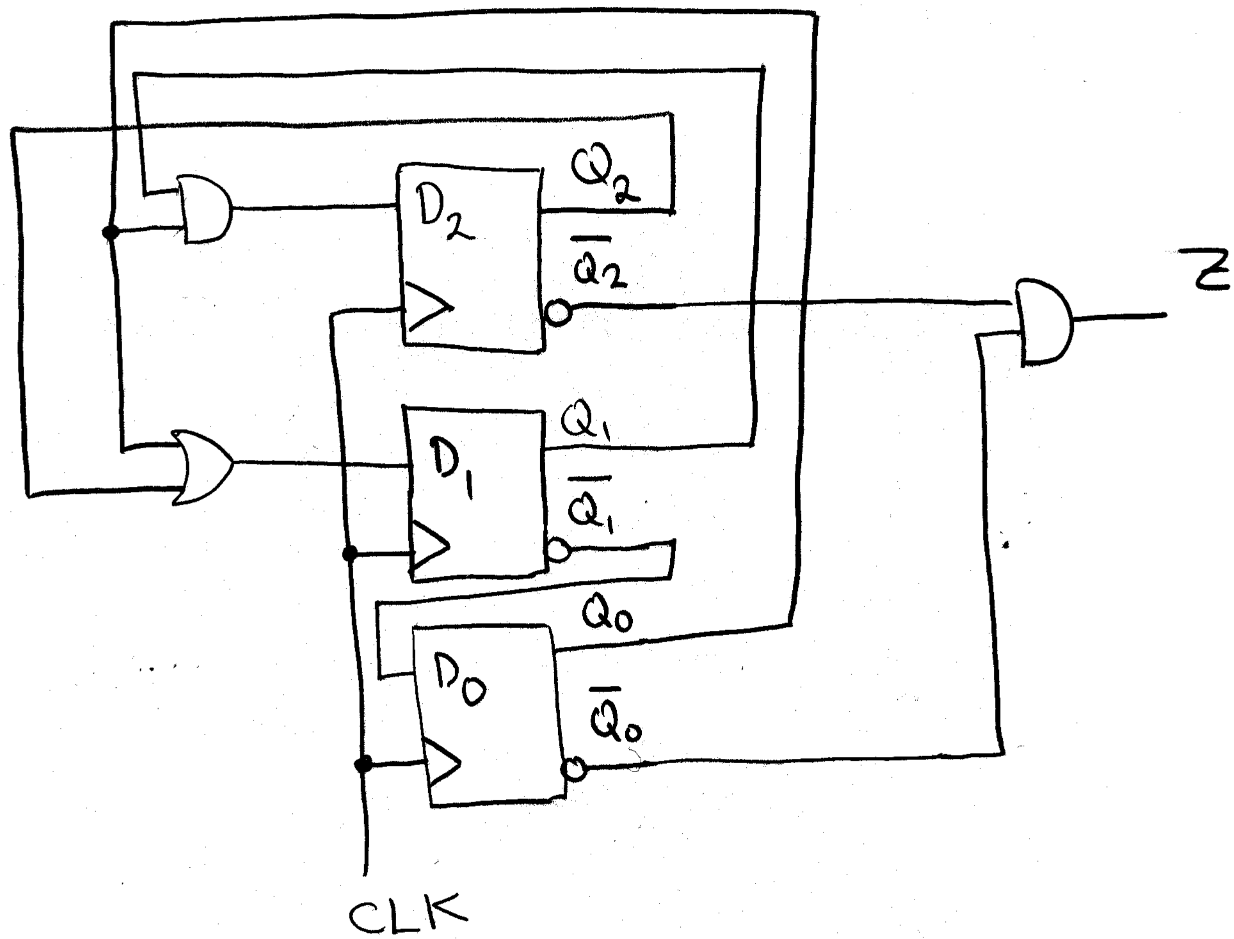
$z = \overline{Q_2}\,\overline{Q_0}$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	1	1	0	0
1	X	X	X	0

$D_0^+ = \overline{Q_1}$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	1	0	0	1
1	X	X	X	0

1(d)



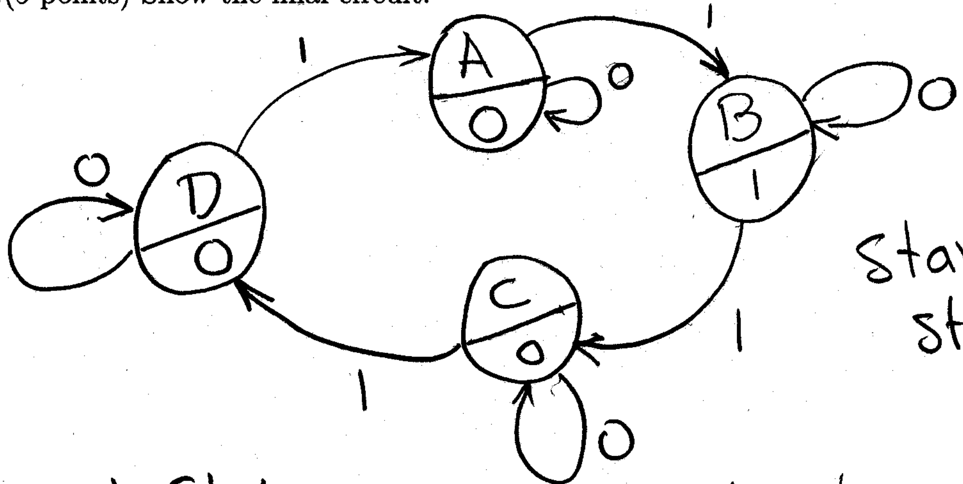
2-1
/2

Problem 2 (25 points total)
We want to build a Moore circuit that outputs a 1 if the number of 1s received can be expressed as $4k+1$ where $k = 0, 1, \ldots$ is an integer.
As an example, consider the following input/output sequence:

Input: 001111100
Output: 0001000100

Note that in this Moore circuit, after the first 1 is received, the output becomes 1 in the next clock cycle. Then the output becomes 1 after four more 1s have been received.
2(a)(5 points) Give the Moore state diagram for this problem.
2(b)(10 points) Derive the state table for implementing the circuit using D flip-flops.
2(c)(5 points) Use K-maps to compute optimal expressions for the inputs to the D flip-flops.
2(d)(5 points) Show the final circuit.

2(a)



Starting state: A.

2(b)

Present State $Q_1 Q_0$	Next State ($D_1 D_0$) X=0	X=1	Output
A: 00	00	01	0
B: 01	01	11	1
C: 11	11	10	0
D: 10	10	00	0

Next state and D-Flip-flop input equations are the same.

2(c)

Q_1Q_0 \ X	0	1
00	0	0
01	0	1*
11	1	1
10	1*	0

$D_1 = Q_0X + Q_1\overline{X}$

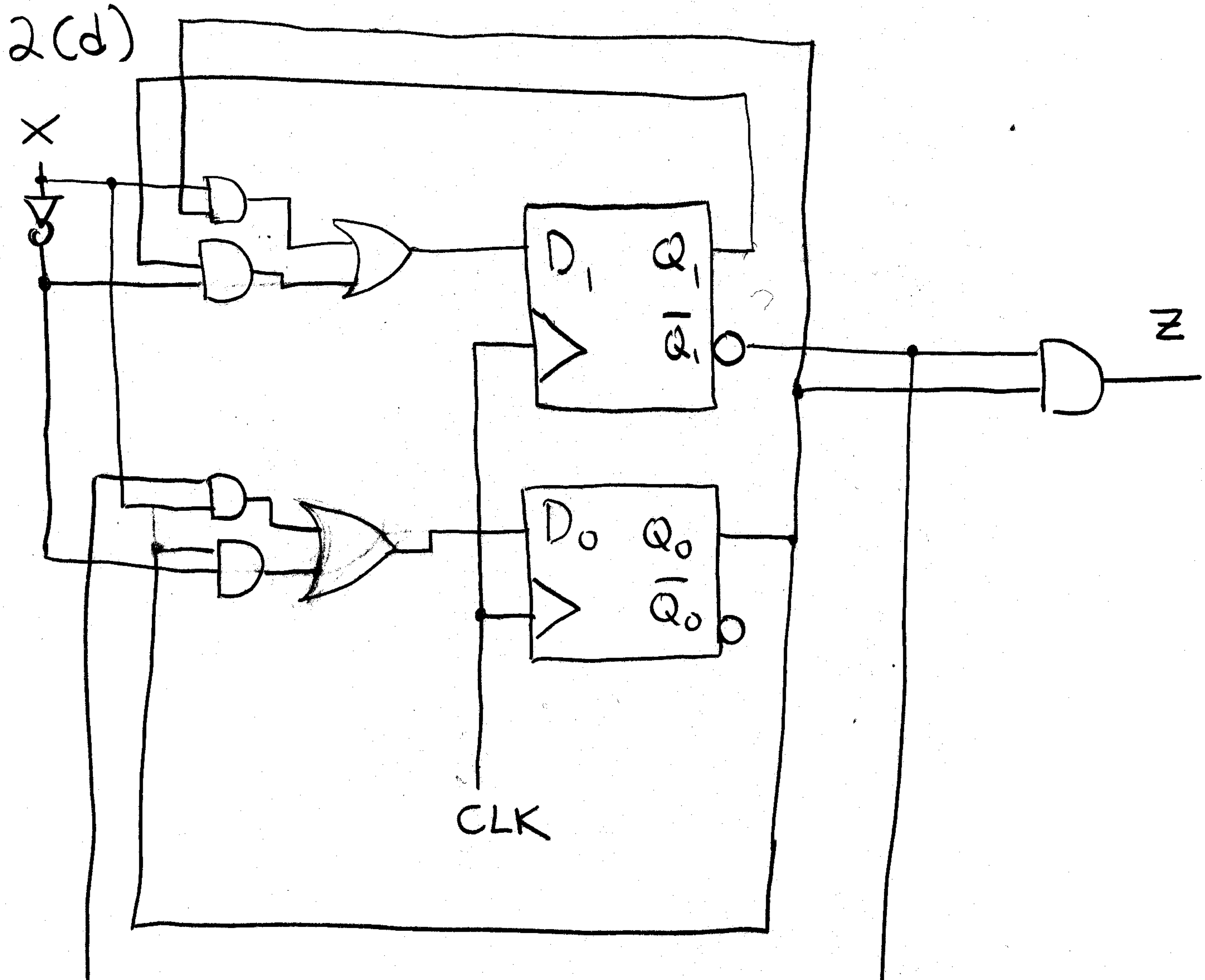
Q_1Q_0 \ X	0	1
00	0	1*
01	1	1
11	1*	0
10	0	0

$D_0 = \overline{Q_1}X + Q_0\overline{X}$

Q_1 \ Q_0	0	1
0	0	1
1	0	0

$Z = \overline{Q_1}Q_0$

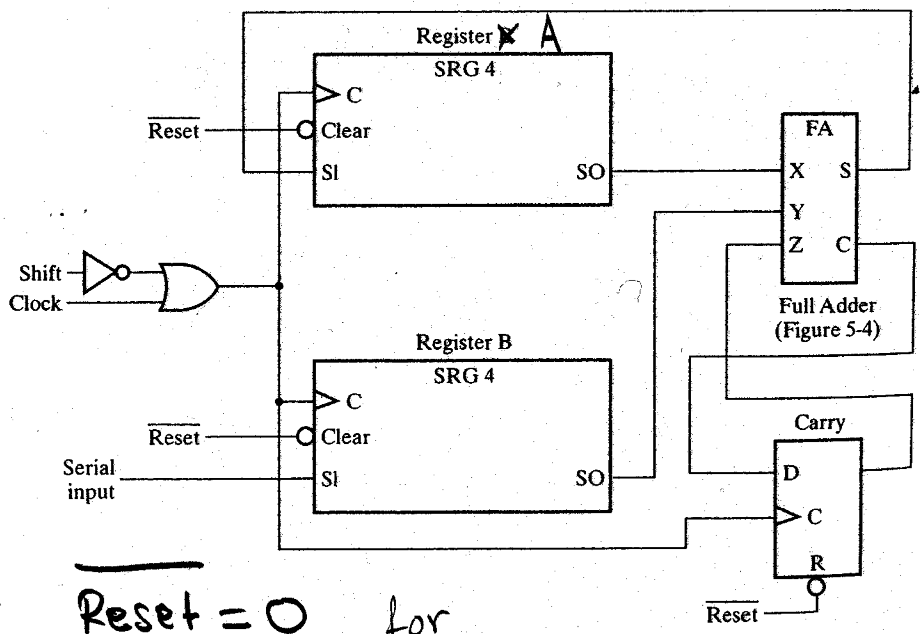
2(d)



3-1
3

Problem 3 (30 points total)
We would like to use the serial adder circuit below to add: 2 − 1. We also want to modify the circuit as described below.
3(a)(**5 points**) Indicate how to initialize the registers and the carry to zero.
3(b)(**10 points**) Indicate how to use the inputs to compute 2 − 1.
For full credit, you will need to show:

- **values of all inputs**
- **the states of registers** A**,** B **and the Carry, with respect to the rise of the clock**
- **if the states of the registers or the Carry cannot be determined, simply mark them with X.**



3(a) Set $\overline{\text{Reset}} = 0$ for Carry, Registers A & B.

3(b)

	SI	Reg B	Reg A	Carry
2	0	0000	0000	0
	1	0000	0000	0
	0	1000	0000	0
	0	0100	0000	0
−1	1	0010	0000	0
	1	1001	0000	0
	1	1100	1000	0
	1	1110	0100	0

*Changes occur after next ↑

* Shift = 1 for all clock periods. (Shift=0 at end)

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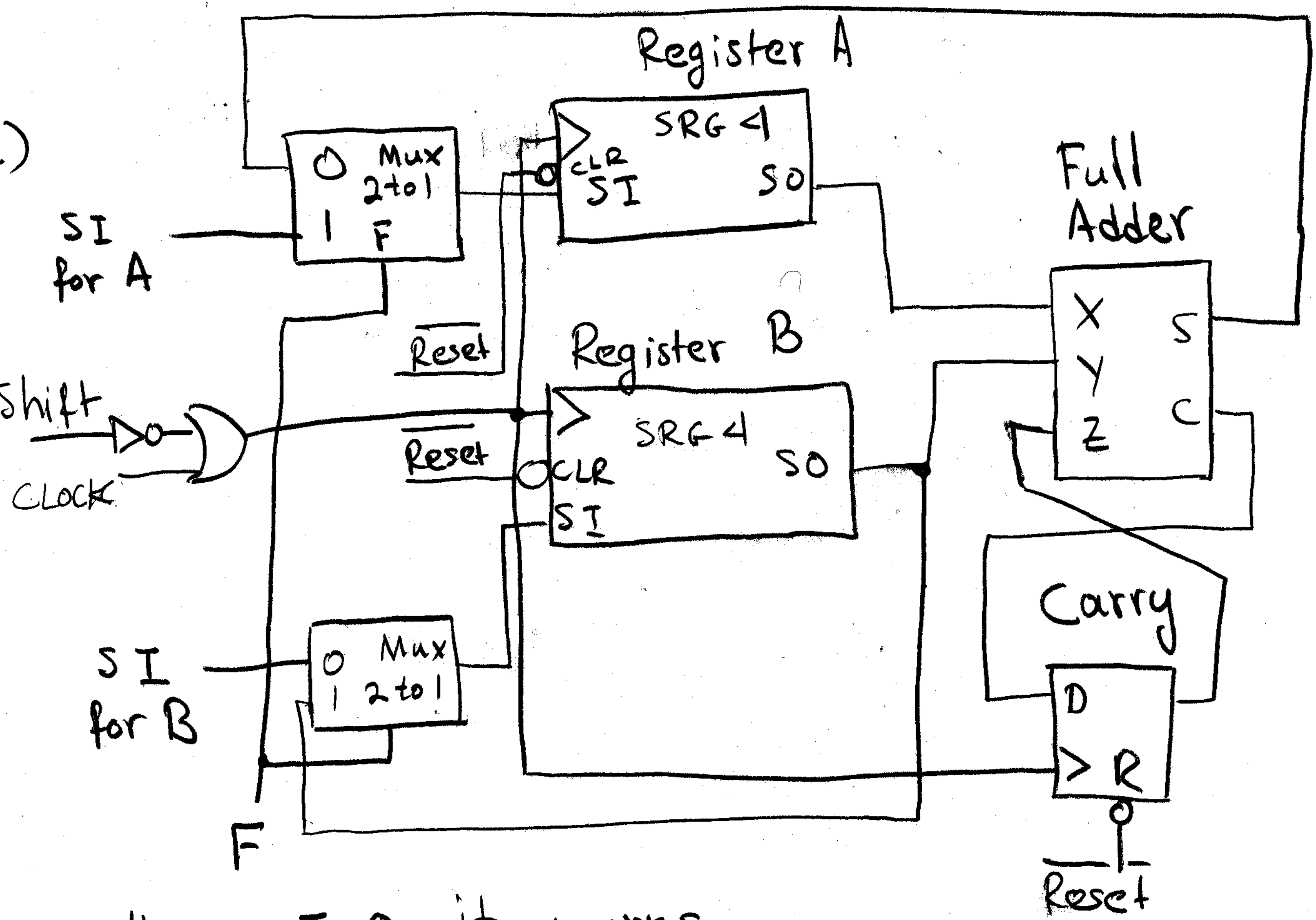
We need four more ↑s:

SI	Reg B	Reg A	Carry
0	1111	0010	0
0	0111	1001	0
0	0011	0100	1
0	0001	0010	1
	0000	0001	1

shift=0

3(e)



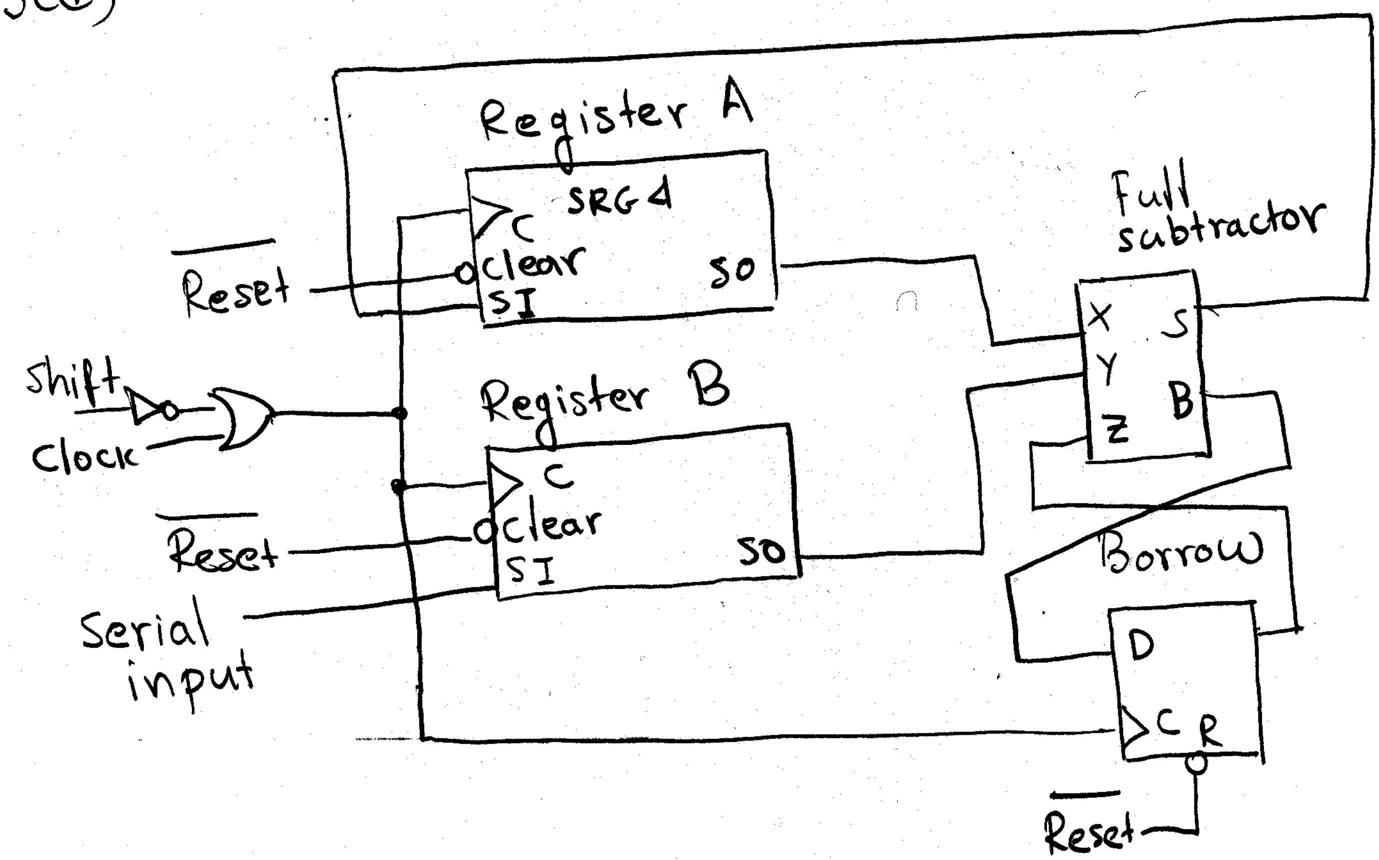
* When F=0, it works as before.
* When F=1, A gets SI and B gets its value shifted back in.

3

3(c)(**2 points**) Please indicate when we need to reset the Carry bit to zero.
3(d)(**5 points**) Suppose that we want to modify the circuit for performing subtractions. That is assume that we want to compute $A - N_1 - N_2 - \ldots$. Indicate how you will have to modify the circuit to do this.
3(e)(**8 points**) Suppose that we want to modify the circuit so that A can either: (i) store the result of the addition, as it is setup right now, or (ii) load in a new value into A, while leaving B unchanged. Indicate how this can be accomplished in 4 cycles.
Hint: Use two 2-to-1 multiplexers and any additional logic (if needed) to accomplish the task.

3(c) The Carry should be reset to zero every four cycles (after each addition).

3(d)



3(e) See page 3-2.

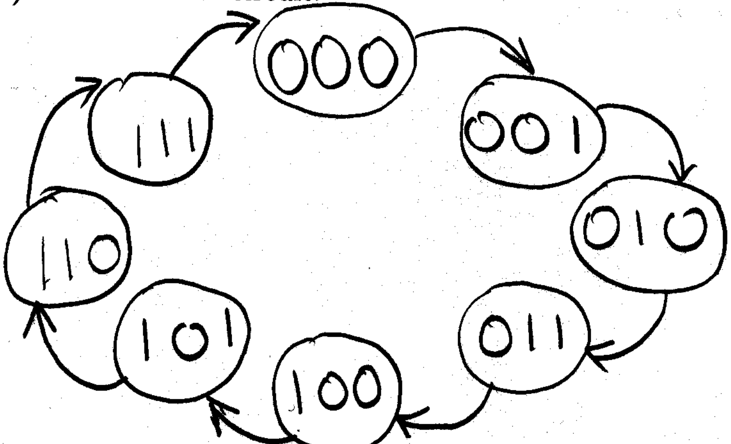
4 - 1/2

Problem 4 (25 points total) Design a binary counter that counts from 0 to 7:

0, 1, 2, 3, 4, 5, 6, 7 and then the counting repeats.

4(a)(**5 points**) Draw the state transition diagram.
4(b)(**10 points**) Derive the state table for implementing the counter using D Flip-Flops.
4(c)(**5 points**) Use K-maps to minimize the inputs to the D Flip-Flops.
4(d)(**5 points**) Show the final circuit.

4(a)



4(b)

Present state $Q_2Q_1Q_0$	Next state / Flip-Flop Inputs $Q_2^+Q_1^+Q_0^+$ / $D_2D_1D_0$
0 0 0	0 0 1
0 0 1	0 1 0
0 1 0	0 1 1
0 1 1	1 0 0
1 0 0	1 0 1
1 0 1	1 1 0
1 1 0	1 1 1
1 1 1	0 0 0

4(c)

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	0	1	0
1	1	1	0	1

$$D_2 = \overline{Q_2}Q_1Q_0 + Q_2\overline{Q_0} + Q_2\overline{Q_1}$$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	0	1	0	1
1	0	1	0	1

$$D_1 = \overline{Q_1}Q_0 + Q_1\overline{Q_0}$$

$Q_2 \backslash Q_1Q_0$	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$$D_0 = \overline{Q_0}$$

4(d)