



□ FIGURE 7-8
Memory Unit Connected to Address and Data Buses

This is a write operation with A_1 supplying the address. Note that the statement does not specify the buses explicitly. Nevertheless, it implies that required select inputs for the address bus decoder are 01 (for A_1), the select inputs for the data bus source decoder are 10 (for D_2), and the select inputs for the data bus destination decoder are 11 (for Memory Write).

The read operation in a memory with buses can be specified similarly. The statement

$$\text{Read: } D_1 \leftarrow M[A_2]$$

specifies a read operation from the memory word having the address given in register A_2 . The data from memory is transferred to register D_1 . The statement implies that the select inputs for the address bus decoder are 10 (for A_2), the select

inputs for the
inputs for the
In the
logic, the ad
clock cycles.
multiple clo
the read is s
ory operatio

7-6 DA

Instead of I
computer sy
shared oper
a microoper
inputs of the
operation is
circuit, the e
ALU, and in
shift operati
tions are als

Recall
interconnect
cerned with
ALU is und
binational c
words, and i

The da
of a comput
that implem
multiplexers
are included
more buses.
as in the per
datapath wi
shading and
7-9. The bla
Each registe
buses A and
correspondin
constants ca
Data out, to
such as mem
address info