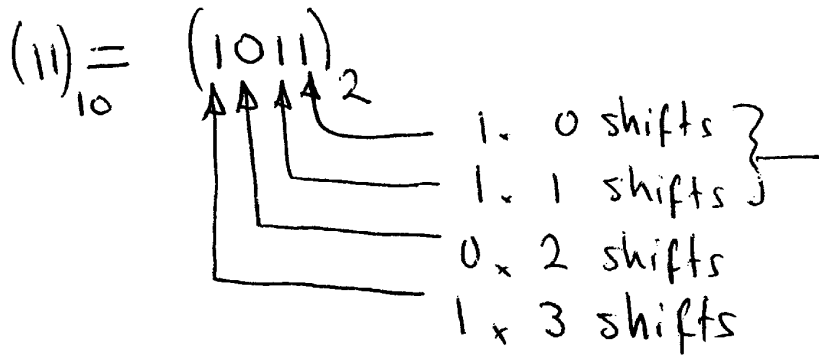


Final Exam Practice Problems

1. Show the microcode for multiplying R_1 by 11.



$$R_2 \leftarrow R_1$$

$$R_3 \leftarrow sl R_1$$

$$R_2 \leftarrow R_2 + R_3$$

$$R_1 \leftarrow sl R_1$$

$$R_1 \leftarrow sl R_1$$

$$R_1 \leftarrow sl R_1$$

$$R_1 \leftarrow R_1 + R_2$$

1. 3 shifts

2. Set the 4th, 5th, 6th bits of CR to 1, 1, 0.

To set bits to 1, use \vee (OR)

To set bits to 0, use \wedge (AND).

$$CR \leftarrow CR \vee \underbrace{(1100000)}_{\substack{6th \ 5th \ 4th}}_2$$

$$CR \leftarrow CR \wedge \underbrace{(11\dots101111)}_{\substack{\text{all 1s} \ 4th}}_2$$

3. Three-state Bus Problem (Figure 7-7c in book)²
 show the μ code for: (attached)

$$R_0 \leftarrow R_2, R_1 \leftarrow R_1$$

Note: The \leftarrow means we are supposed to do this concurrently. But, we cannot drive the bus with both the contents of R_1 & R_2 .

∴ We must ignore $R_1 \leftarrow R_1$ (no use anyway)

For $R_0 \leftarrow R_2$:

Enables			Loads		
E_2	E_1	E_0	L_2	L_1	L_0
1	0	0	0	0	1

\uparrow
 R_2 is driving the bus

\uparrow
 R_0 will load from the bus.

4. Address/Data bus problem (figure 7-8 in book)

Assume that:

$$A_0 = 1000, A_1 = 100, A_2 = 10$$

$$D_0 = 5, D_1 = 2, D_2 = 1$$

4 (a) Indicate control signals for:

$$M[10] \leftarrow 5$$

Address Decoder:

0: 0
 1: 0
 2: 1 \leftarrow for A_2

Data bus Source Decoder

0: 1 \leftarrow use D_0 as the source.
 1: 0
 2: 0
 3: 0 \leftarrow No Read

Data bus Destination Decoder:

0: 0
1: 0
2: 0
3: 1 write to memory

$$(b) \quad D_2 \leftarrow M[100]$$

Address Decoder Data bus Source Decoder

0: 0
1: 1 ← use A_1
2: 0

0: 0
1: 0
2: 0
3: 1 ← read from memory.

Data bus Destination Decoder

0: 0
1: 0
2: 1 ← D_2
3: 0 no write

5. Datapath problem (Figure 7-9 in book)

$$5(a) \quad R_3 \leftarrow R_1 - R_3$$

Note: The subtraction has to be executed by the ALU

We will put R_1 on bus A, R_3 on bus B.

Steps: 1. A select 1, for placing R_1 on bus A.

B select 3, for placing R_3 on bus B.

MB select 0 for giving R_3 to ALU

2. Set S_2, S_0 & C_{in} to the bit values required for subtraction.

3. MF select = 0 for bringing out ALU result.
MD select = 0 for using MUX F output

Destination select = 3 for R_3

Load enable = 1 for loading R_3

5(b) $R_1 \leftarrow sl R_2$

Note: The shift must be executed by the shifter unit.

\Rightarrow We have to place R_2 on Bus B.

1. B select = 2 for R_2 to bus B

MB select = 0 for R_2 to bus B

2. It select = bits selecting left-shift by 1.

3. MF select = 1 for shifter,

MD select = 0 for MUX F output.

Destination Select = 1 for R_1

Enable = 1 for loading R_1

6. (a) $s_0 = s_1 = 1$, $D_3 D_2 D_1 D_0 = (0111)_2$

$s_1 s_0 = 11 \Rightarrow$ rotate 3 times (left).

$(0111) \leftarrow = 1110$

$(1110) \leftarrow = 1101$

$(1101) \leftarrow = \underline{\underline{1011}}$

(b) $s_1 s_0 = 10$. means 2

rotations only.

Answer = $(1101)_2$

Problem #6

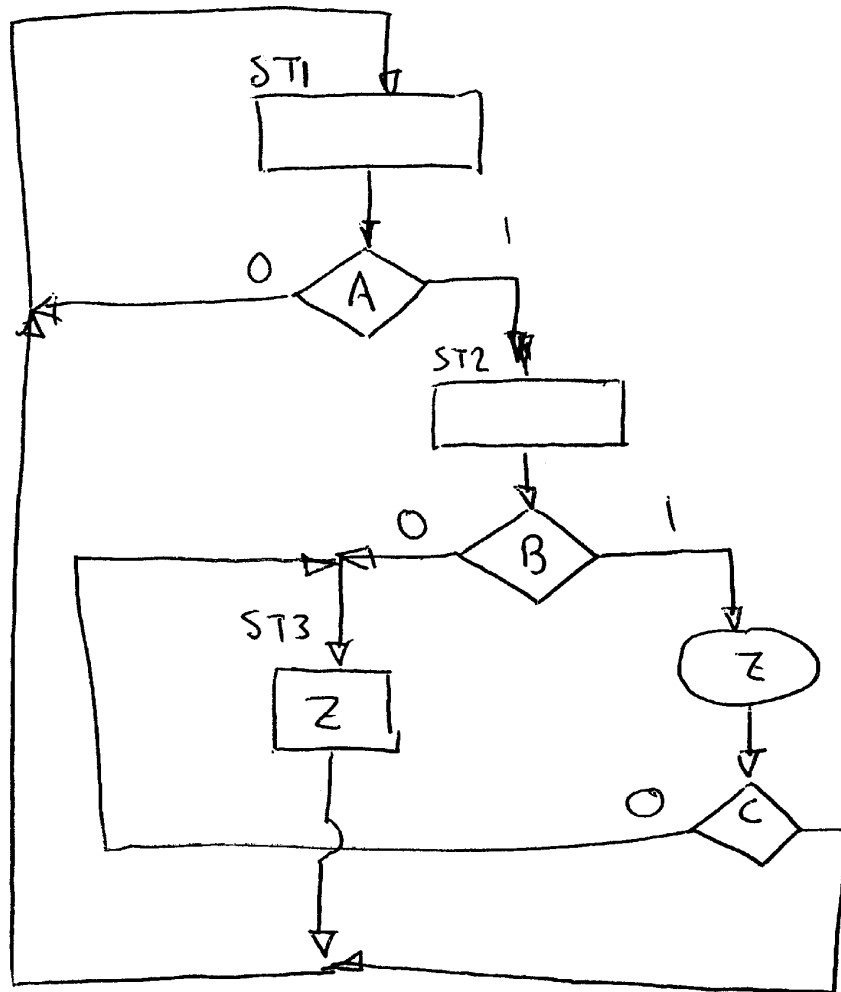
Barrel-Shifter, Fig. 7-17 in text.

6(a) Suppose: $s_0 = s_1 = 1$. $D_3 = 0, D_2 = 1, D_0 = 1$

Give Y_3, Y_2, Y_1, Y_0 .

6(b) Repeat for $s_0 = 0, s_1 = 1$.

8.2

from
book.

1. states: ST1, ST2, ST3

2. Inputs: A, B, C

3. Outputs: Z

Assume: (i) initial state = ST1.

(ii) Inputs are: given in table below.

Compute: (i) next state &
(ii) output.

A	0	1	1	0	1	1	
B	1	1	1	1	0	0	
C	0	1	0	1	0	1	
State	ST1	ST1	ST2	ST3	ST1	ST2	ST3
Z	0	0	1	1	0	0	1

State Table:

Present State	Inputs A B C	Next state	Output
ST1	0 x x	ST1	0
	1 x x	ST2	0
ST2	x 0 x	ST3	0
	x 1 0	ST3	1
	x 1 1	ST1	1
ST3	x x x	ST1	1

Problem . . . Multiply 11001100 by 1001. 6
0
 using the Multiplier circuit of Figure 8-6. Show
 the first 5 steps.

1. $C \leftarrow 0, A \leftarrow 0, P \leftarrow 7$

2. $Q \leftarrow 1001, B \leftarrow 11001100$

3. $z_0 == 1$

$\Rightarrow A \leftarrow A + B$
 $C \leftarrow \text{cout}$

Yields: (i) 11001100 for A
 (ii) 0 for Cout

4. $C \leftarrow 0, C \parallel A \parallel Q \leftarrow \text{sr } C \parallel A \parallel Q$

yields: $C = 0$
 $A = 01100110$
 $Q = 0000 \ 0100$

$P \leftarrow P - 1$ yields $P = 6$.

5. $z == 1$ fails since $7 \neq 0$

⋮

... in class.