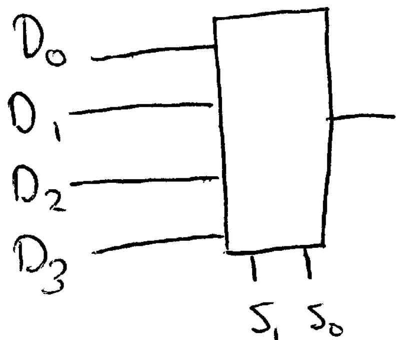
3-7
MUX

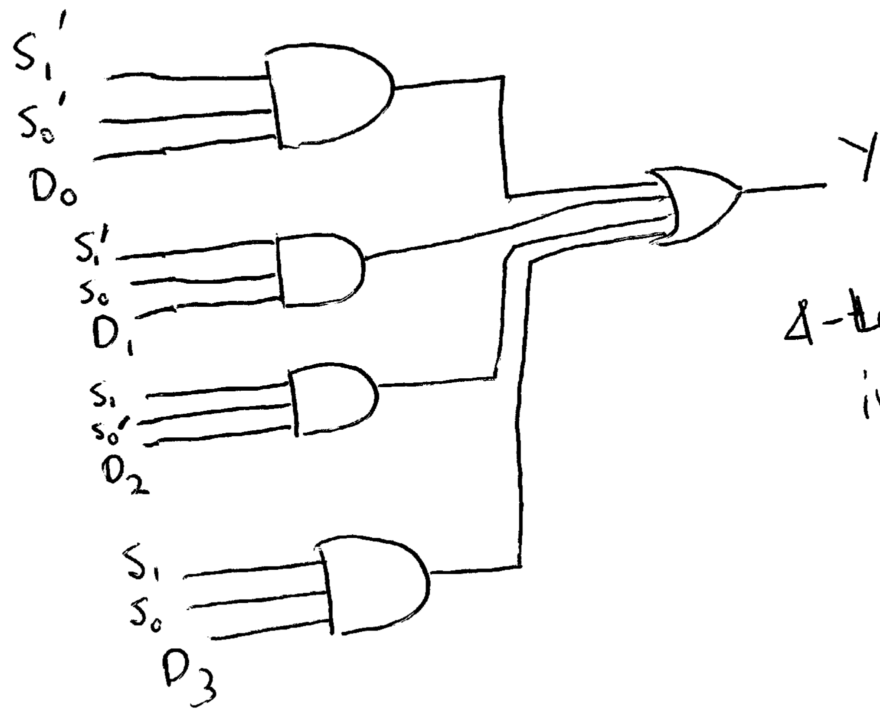
(p 119) Multiplexers

4-to-1 Line Multiplexer.

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



select the input that is transmitted to Y.



4-to-1 Mux implementation.

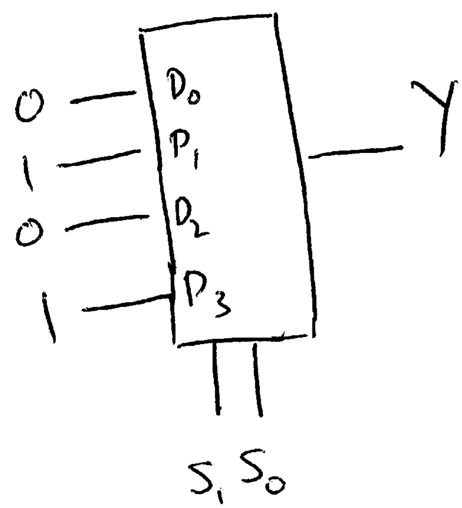
Muxs can be used to implement Logic functions.

→ A 2-variable function can be implemented by a 2^2 to 1 Mux & 0,1 inputs

Eg:

S_1	S_0	Y
0	0	$D_0 = 0$
0	1	$D_1 = 1$
1	1	$D_2 = 0$
1	0	$D_3 = 1$

Soln:



→ A 3-variable function can be implemented by: (a) a 2^2 to 1 Mux & two inputs set to the S_0, S_1 and the other variable at $D_0 - D_3$; ~~or~~

(b) a 2^3 to 1 Mux & inputs set to S_0, S_1, S_2 inputs.

- Eg:

A	B	C	Y	
0	0	0	0	$D_0 = C$
0	0	1	1	
0	1	0	0	$D_1 = 0$
0	1	1	0	
1	0	0	1	$D_2 = C'$
1	0	1	0	
1	1	0	1	$D_3 = 1$
1	1	1	1	

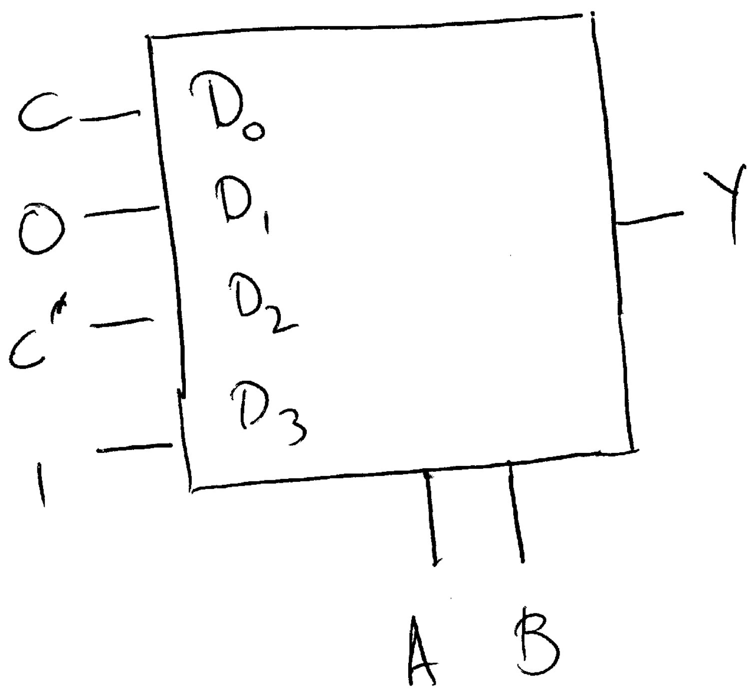
Use any 2 out of 3 as selectors.
Use last one for input.

Eg: for $AB = 00$, D_0 input is:

$$\left.\begin{array}{ll} D_0 = Y = 0 & \text{for } C = 0 \\ D_0 = Y = 1 & \text{for } C = 1 \end{array}\right\} \Rightarrow D_0 = C$$

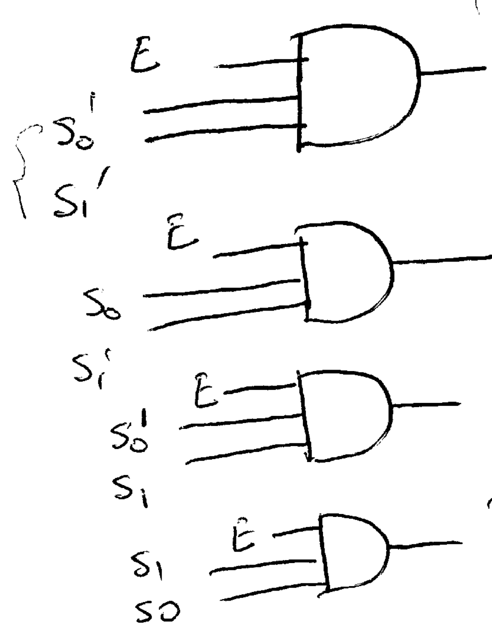
similarly (see above).

Soln



p12a: DeMux = Decoder + Enable.

1-4 DeMux: Demultiplexer performs the inverse of the multiplexing operation: that is, a demultiplexer receives information from a single line and transmits it to one of 2^n possible output lines.



$D_0 = E S_0' S_1'$ 00

$D_1 = E S_0 S_1'$ 01

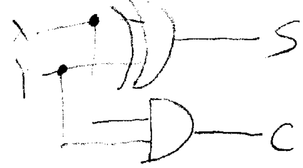
$D_2 = E S_0' S_1$ 10

$D_3 = E S_1 S_0$ 11

n selection lines

2^n

→ See back!!



Half Adder

A half adder is an arithmetic circuit that generates the sum of two binary digits.

Diagram on P126.

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = \bar{X}Y + X\bar{Y} = X \oplus Y$

$C = XY$

X \ Y	0	1
0		
1		1

$C = XY$

X \ Y	0	1
0		1
1	1	

$S = X \oplus Y$

Full Adder

A full adder is a combinational circuit that forms the arithmetic sum of three input bits.

X, Y represent the two significant bits to be added — Z represents the carry from the previous lower significant position.

Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

X \ YZ	00	01	11	10
0		1		1
1	1		1	

$S = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ = X \oplus Y \oplus Z$

X \ YZ	00	01	11	10
0			1	
1		1	1	1

$\rightarrow XY$

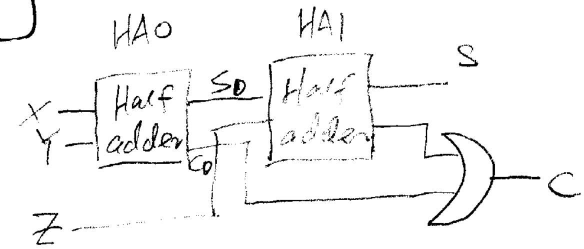
$C = XY + XZ + YZ$
$= XY + Z(X\bar{Y} + \bar{X}Y)$
$= XY + Z(X \oplus Y)$

In general, $Z(X+Y) \neq Z(X\bar{Y} + \bar{X}Y)$

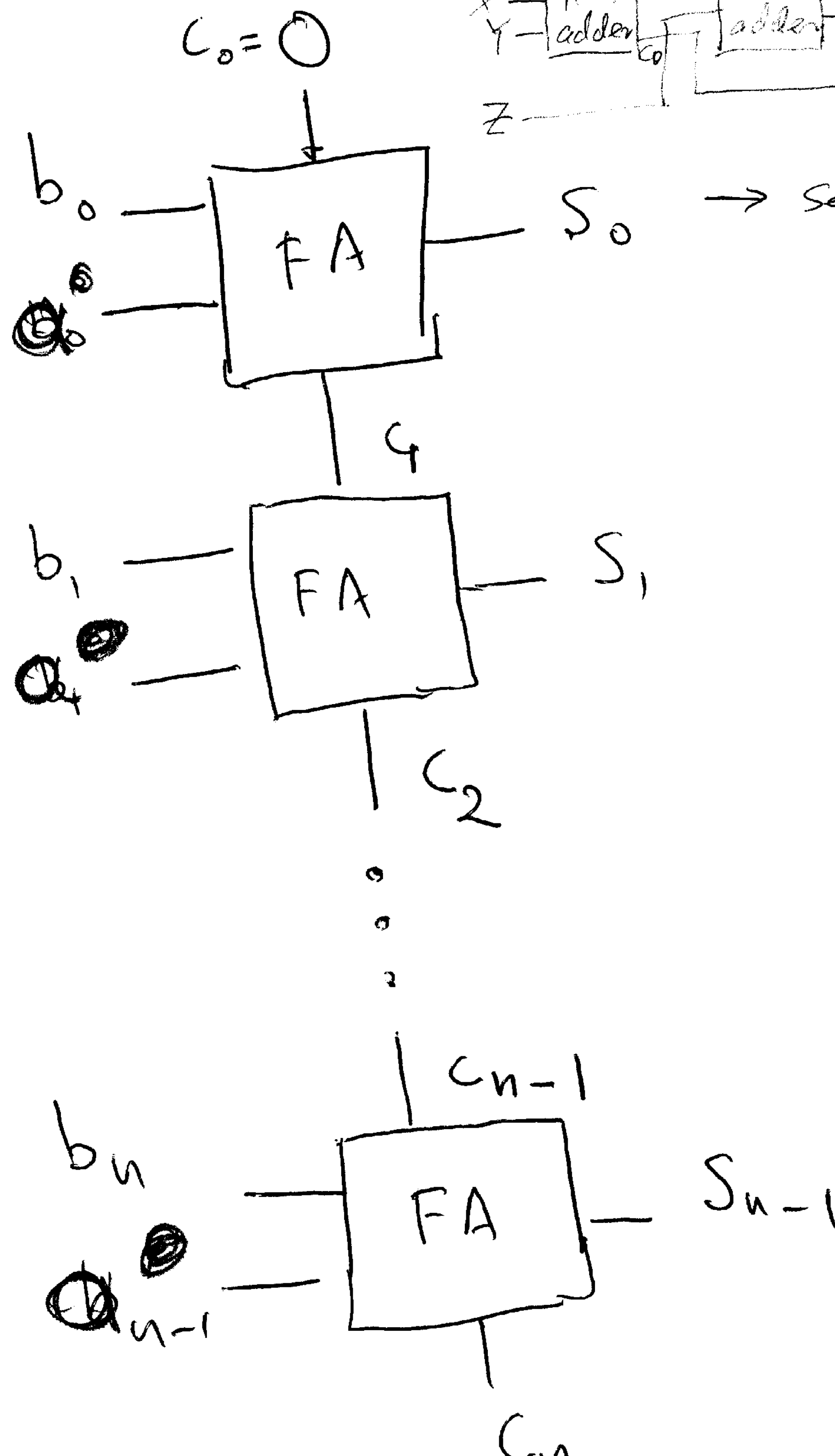
Share $X \oplus Y$. P127

Two half adder $\Rightarrow$ Full adder $\rightarrow$ See next page.

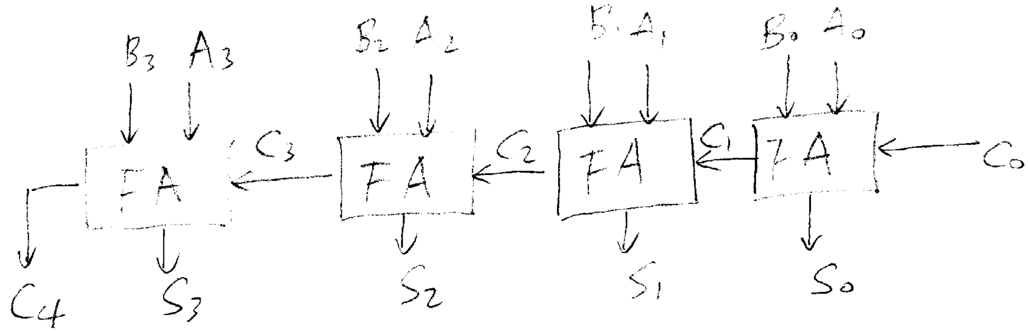
Full-Adders can be cascaded into a Ripple carry ~~adder~~ adder (p128)



→ see back!!



But they are slow


B3 A3
B2 A2
B1 A1
B0 A0
FA
FA
FA
FA
C3
C2
C1
C0
C4
S3
S2
S1
S0