

Mealy versus Moore

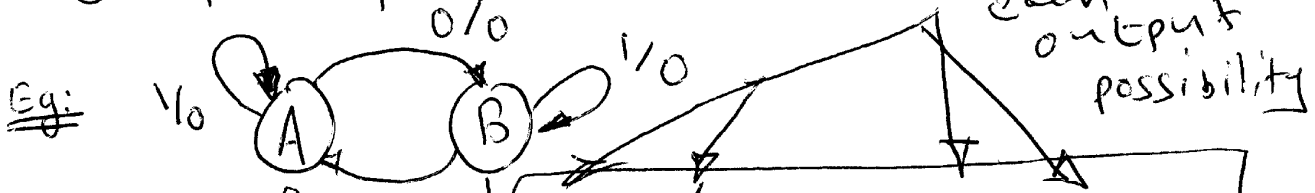
pi99
↳ Memorize Me

Figure 5-5

Mealy design

→ Output depends on both inputs and the current state.

→ On your state table, you need rows for each possible state and columns for each possible input.



Current State	Next state		Output		D	Input FF $I=1$
	I=0	I=1	I=0	I=1		
A	B	A	0	0	1	0
B	A	B	1	0	0	1

→ Note that k-maps use both the Input & current state.

Eg: Assign A to 0
Assign B to 1

DO NOT USE A, B for the k-maps!

These are the states, they correspond to Φ .

D Flip-Flop Input Map

Current-State (s) Q / \bar{Q} Input(s) \bar{I} I

\bar{Q} 0	1	0
Q 1	0	1

$$D = Q'I' + QI$$

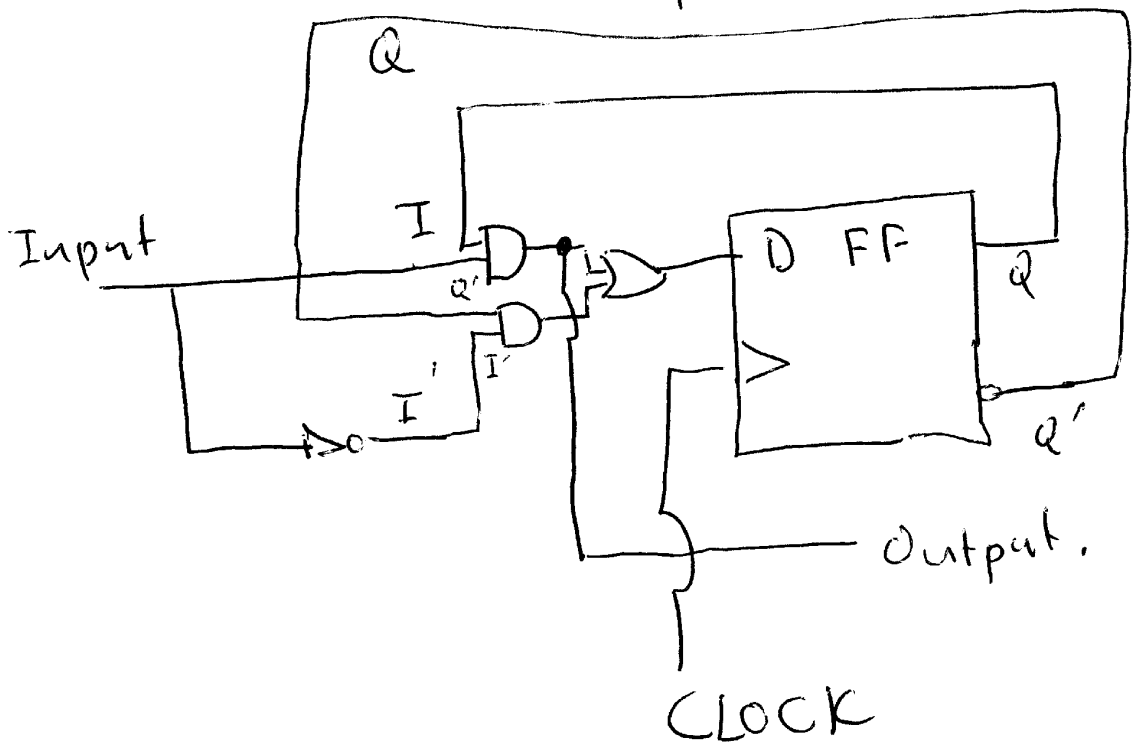
Output

Current-State (s) Q / \bar{Q} Input(s) \bar{I} I

\bar{Q} 0	0	0
Q 1	1	0

$$\text{Output} = QI + Q'\bar{I}$$

Circuit



→ Note that the output
- changes with the input.

→ It does not wait for the
clock.

⚠ For (4-21), based on the
given timing diagram of page
243, only a Mealy solution
can be given.

Disadvantage:

If the input changes during
the clock period, so does
the output (during the period).

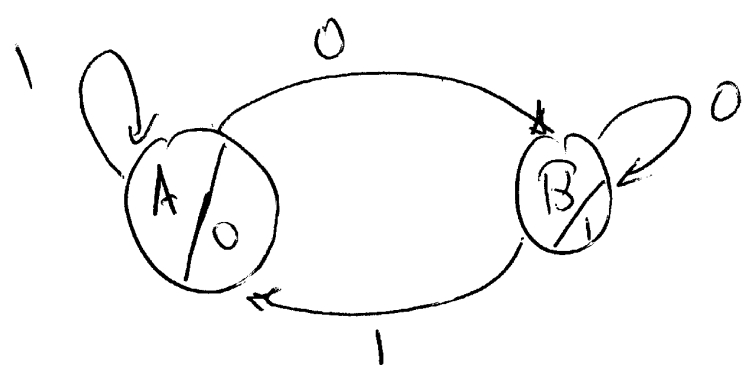
So, it does not meet the specification
of staying at 1 ($E=1$) after an error.

⇒ Solution in class is better (?)

Moore Design

- Output only depends on the current state.
- On your state table, you:
 - only need one column for the output
 - still need columns for each possible input for the next state.

Eq.



Use T-FFs, Assign $A=0, B=1$.

Current state
 $A=0$
 $B=1$

Next State
 $I=0 \quad I=1$
 $B=1 \quad A=0$
 $B=1 \quad A=0$

output
 0
 1
 ↑

T-FF input
 $I=0 \quad I=1$
 1 0
 0 1

one column.

k-map(s) for Next State

Current State(s) Q

	Input(s) I	
0	0	1
1	0	1

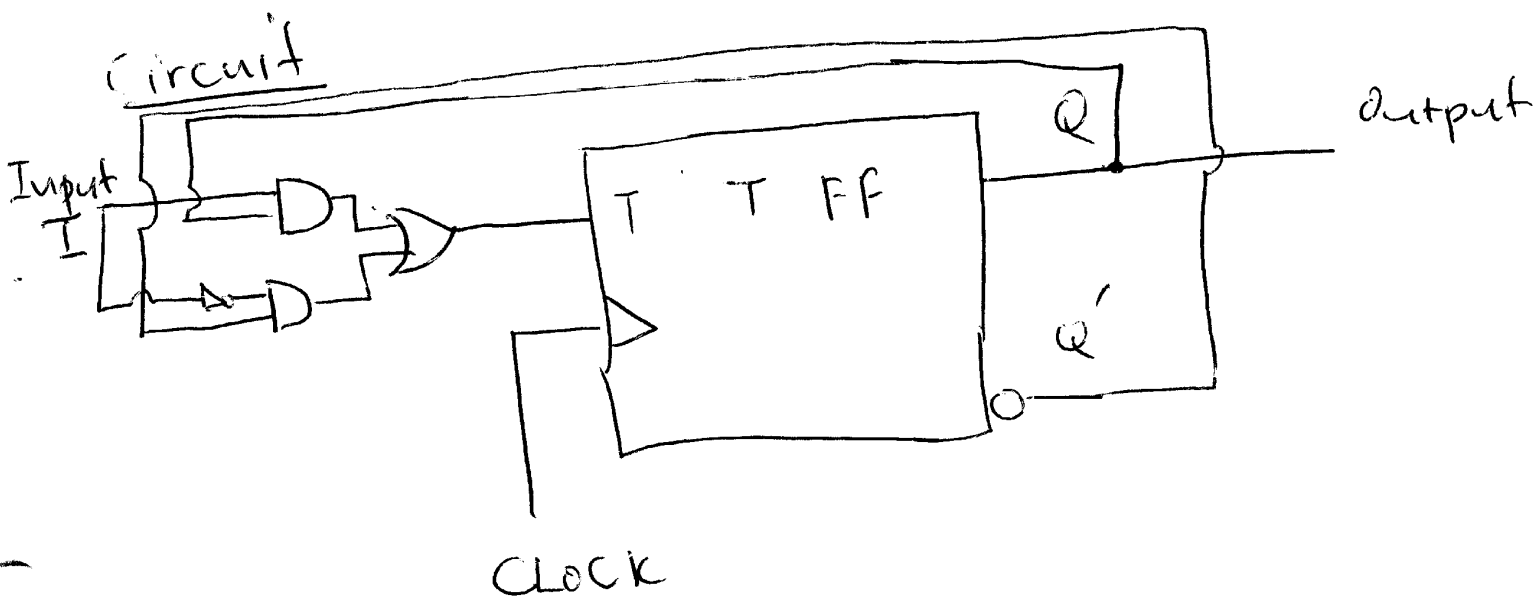
T-FF input = $QI + Q'I'$

k-map(s) for output

Current State(s) Q

0	0
1	1

output = Q .



NOTE: Output changes AFTER Input on \uparrow .

tes a more advanced problem and the asterisk (*) indicates a
 in the Prentice Hall Companion Website Gallery.

usual or computer-based logic simulation similar to that given
 for the SR latch shown in Figure 4-6. Construct the input
 ping in mind that changes in state for this type of latch occur in
 rather than 1.

usual or computer-based logic simulation similar to that given
 for the SR latch with control input C in Figure 4-7. In
 amine the behavior of the circuit when S and R are changed
 re value 1.

shown in Figure 4-8 can be constructed with only four NAND
 be done by removing the inverter and connecting the output
 NAND gate to the input of the lower gate. Use manual or
 ed logic simulation to show that the new circuit is functionally
 e original one.

gic diagram of the D latch shown in Figure 4-8, using NOR

gic diagram of the SR master-slave flip-flop in Figure 4-10,
 gates only.

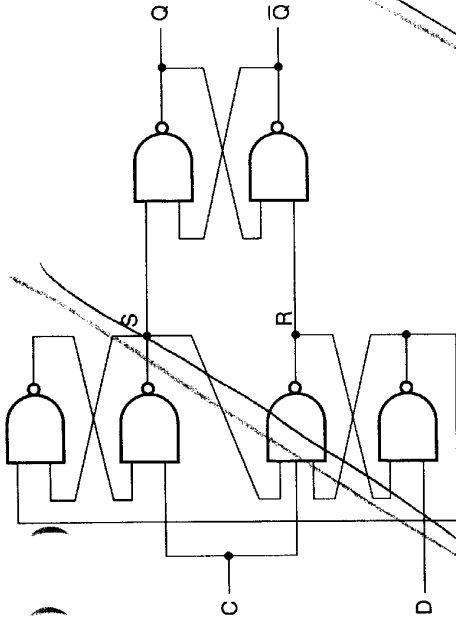
ing diagram similar to Figure 4-11 for a JK master-slave flip-
 ir clock pulses. Show the timing signals for C, J, K, Y, and Q.
 initially the output Q is equal to 1 with the first pulse J = 0 and
 or successive pulses, J goes to 1 followed by K going to 0 and
 ack to 0. Assume that each input changes after the negative
 lse.

m 4-6, using a positive-edge-triggered JK flip-flop. Show the
 is for C, J, K, and Q.

rnative design for a positive-edge-triggered D flip-flop is
 e 4-35. Simulate the circuit to determine whether its
 avior is identical to that of the circuit in Figure 4-13.

ulation to compare the master-slave JK flip-flop in
 h a negative-edge-triggered JK flip-flop which is identical to
 gure 4-14, except that the inverter on the clock input C to the
 ed. Apply waveforms that demonstrate the difference in
 se two circuits for changes in the J and K inputs while C = 1.

ristic equations for each type of flip-flop, using the
 Table 4-1. A characteristic equation gives the function



□ FIGURE 4-35
 Circuit for Problem 4-8

$Q(t+1)$ in terms of $Q(t)$ and the input variables to the flip-flop. Use the
 characteristic equation for the JK flip-flop to find equations $A(t+1)$ and $B(t$
 $+ 1)$ from the flip-flop input equations corresponding to Table 4-4.

4-11. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and
 one output Z is specified by the following input equations:

$$D_A = \bar{X}Y + XA \quad D_B = \bar{X}B + XA \quad Z = XB$$

- (a) Draw the logic diagram of the circuit.
- (b) Derive the state table.
- (c) Derive the state diagram.

4-12. *A sequential circuit has three D flip-flops A, B, and C, and one input X.
 The circuit is described by the following input equations:

$$D_A = (\bar{B}\bar{C} + \bar{B}C)X + (B\bar{C} + \bar{B}\bar{C})\bar{X}$$

$$D_B = A$$

$$D_C = B$$

- (a) Derive the state table for the circuit.
 - (b) Draw two state diagrams, one for $X = 0$ and the other for $X = 1$.
- 4-13. A sequential circuit has one flip-flop Q, two inputs X and Y, and one output
 S. The circuit consists of a full adder circuit connected to a D flip-flop, as
 shown in Figure 4-36. Derive the state table and state diagram of the
 sequential circuit.

Solve in
 Class

Problem Solutions - Chapter 4

4-10.*

J	K	Q(t)	Q(t+1)	S	R	Q(t)	Q(t+1)	D	Q(t)	Q(t+1)	T	Q(t)	Q(t+1)
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	0	1	0	0	1	1
0	1	0	0	0	1	0	0	1	0	1	1	0	1
0	1	1	0	0	1	1	0	1	1	1	1	1	0
1	0	0	1	1	0	0	1						
1	0	1	1	1	0	1	1						
1	1	0	1	1	1	0	X						
1	1	1	0	1	1	1	X						

$Q(t+1) = D$ $Q(t+1) = T \oplus Q$

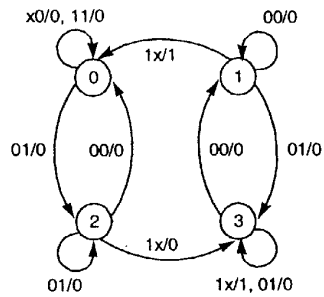
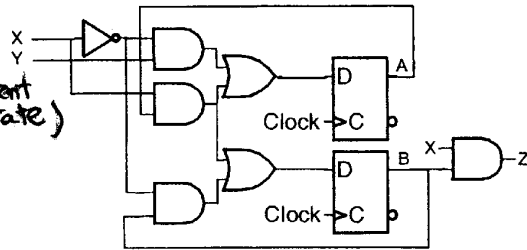
$J_A = B$ $K_A = BX$
 $J_B = \bar{X}$ $K_B = A\bar{X} + \bar{A}X$

$Q(t+1) = J\bar{Q} + \bar{K}Q$ $Q(t+1) = S + \bar{R}Q$

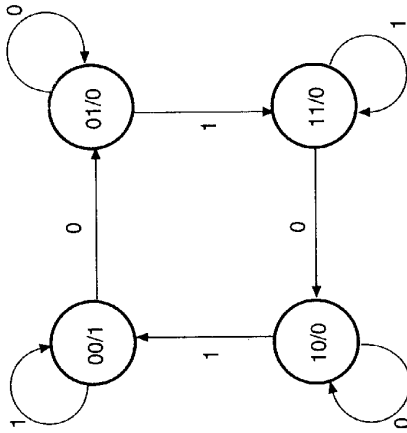
$A(t+1) = J_A\bar{A} + \bar{K}_A A$ = $B\bar{A} + \bar{B}A + XA$
 $B(t+1) = J_B\bar{B} + \bar{K}_B B$ = $\bar{X}\bar{B} + ABX + \bar{A}B\bar{X}$

4-11. Teach in Class

Present state	Inputs		Next state		Output	
A	B	X	Y	A	B	Z
s_0	0	0	0	0	0	0
	0	0	0	1	1	0
	0	0	1	0	0	0
	0	0	1	1	0	0
s_1	0	1	0	0	0	1
	0	1	0	1	1	1
	0	1	1	0	0	0
	0	1	1	1	0	0
s_2	1	0	0	0	0	0
	1	0	0	1	1	0
	1	0	1	0	1	1
	1	0	1	1	1	1
s_3	1	1	0	0	0	1
	1	1	0	1	1	1
	1	1	1	0	1	1
	1	1	1	1	1	1



Format: XY/Z (x = unspecified)



□ FIGURE 4-39

State Diagram for Problem 4-24 and Problem 4-30

the corresponding output digit is to appear during the same clock cycle on output Z. To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y becomes 1 for one clock cycle. Otherwise, Y is 0.

- (a) Find the state diagram for the serial ten's complementer.
- (b) Find the state table for the serial ten's complementer.

4-23. A serial leading 1's detector is to be designed. A binary integer of arbitrary length is presented to the serial leading 1's detector most significant bit first on input X. When a given bit is presented on input X, the corresponding output bits to appear, during the same clock cycle of output Z. As long as the bits applied to X are 0, Z = 0. When the first 1 is applied to X, Z = 1. For all bit values applied to X after the first 1 is applied, Z = 0. To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y becomes 1 for one clock cycle. Otherwise, Y is 0.

- (a) Find the state diagram for the serial leading 1's detector.
- (b) Find the state table for the serial leading 1's detector.

4-24. *A sequential circuit has two flip-flops A and B, one input X and one output Y. The state diagram is shown in Figure 4-39. Design the circuit with D flip-flops.

4-25. *Convert a D-type flip-flop into a JK flip-flop, using external gates. The gates can be derived by means of a sequential circuit design procedure starting from a state table with the D flip-flop output as the present state and its input as the next state and with J and K as circuit inputs.

4-26. A set-dominant flip-flop has set and reset inputs. It differs from a conventional SR flip-flop in that, when both S and R are equal to 1, the flip-flop is set.

- (a) Obtain the characteristic table of the set-dominant flip-flop.

- (b) Find the state diagram for the set-dominant flip-flop by using a J-K flip-flop and inverters.
- (c) Design the set-dominant flip-flop by using a J-K flip-flop and inverters.

4-27. A JN flip-flop has two inputs J and N. Input J behaves like the complement of a JK flip-flop, and input N behaves like the complement of a JK flip-flop (that is $N = \bar{K}$).

- (a) Obtain the characteristic table of the flip-flop.
- (b) Show that, by connecting the two inputs together, the flip-flop behaves like a JK flip-flop.

4-28. Derive an excitation table for the JN flip-flop defined in Problem 4-27.

4-29. Derive the excitation table of the set-dominant flip-flop defined in Problem 4-23.

4-30. *Design a sequential circuit for the state diagram given in Figure 4-39.

4-31. Find the logic diagram for the sequence recognizer circuit given in Table 4-6. Use D flip-flops.

4-32. Do a logic simulation of your design in Problem 4-31. The correct sequence causes the output to go to 1. The input sequence should include all transitions in the state table. The simulation output should include both the state and output Z.

4-33. *Design a sequential circuit with two JK flip-flops A and B. If E = 0, the circuit remains in the same state, and if E = 1, the circuit goes through the state transitions from 00 to 01 to 10 to 11, back to 00, and then repeats.

4-34. *The state table for a twisted ring counter is given in Table 4-14. Its outputs are the uncomplemented flip-flop outputs. Since it has no inputs, it simply goes from state to state on each clock pulse.

□ TABLE 4-14
State Table for Problem 4-31

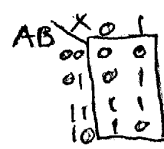
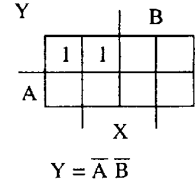
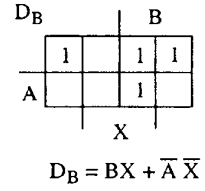
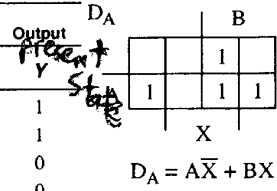
Present State	Next State
ABC	ABC
000	100
100	110
110	111
111	011
011	001
001	000

Problem Solutions - Chapter 4

Search in class

4-24.*

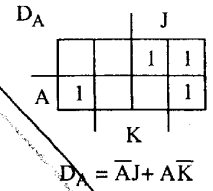
Present state		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	1	1
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	0	0
1	1	1	1	1	0



$D_A = A\bar{X} + BX$

4-25.*

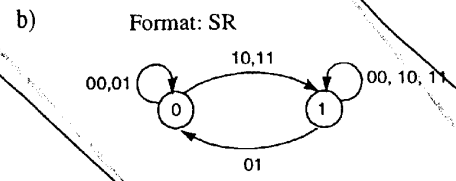
Present state		Input		Next state
A		J	K	A
0		0	0	0
0		0	1	0
0		1	0	1
0		1	1	1
1		0	0	1
1		0	1	0
1		1	0	1
1		1	1	0



4-26.

a)

S	R	Q	
0	0	Q	No Change
0	1	0	Reset
1	0	1	Set
1	1	1	Set



c)

Present state	Input		Next state			
	Q	S	R	Q(t+1)	J	K
0	0	0	0	0	0	x
0	0	0	1	0	0	x
0	0	1	0	1	1	x
0	0	1	1	1	1	x
1	1	0	0	1	x	0
1	1	0	1	0	x	1
1	1	1	0	1	x	0
1	1	1	1	1	x	0

$J = S$
 $K = \bar{S}R$

