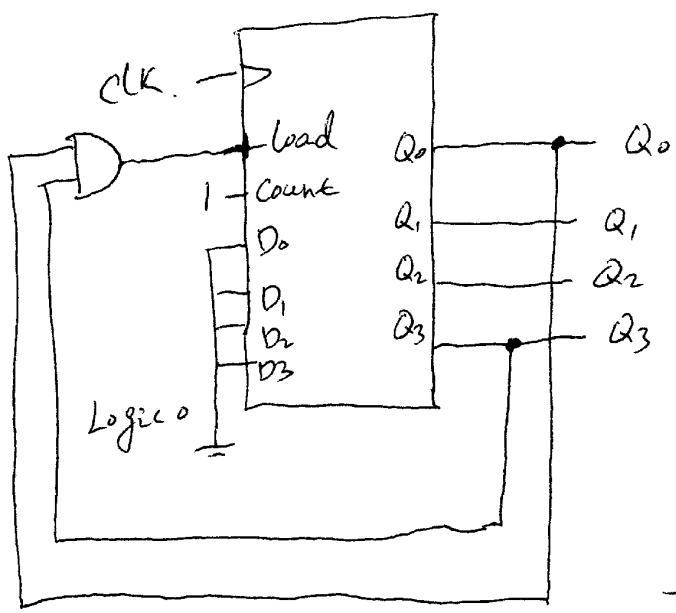


①

The binary counter with parallel load can be converted into a synchronous BCD counter by connecting an external AND gate to it, as shown in Figure 5-13. page 272.



0000
 0001
 0010
 ⋮
 1001
 0000

$Q_0 = Q_3 = 1 \quad \text{Load} = 1$

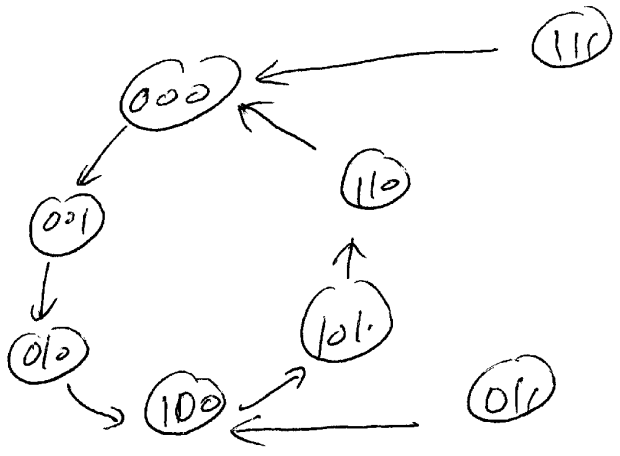
So, on the next clock transition, the counter does not count, but is loaded from its four inputs.

5-6. Other Counters.

BCD Counter

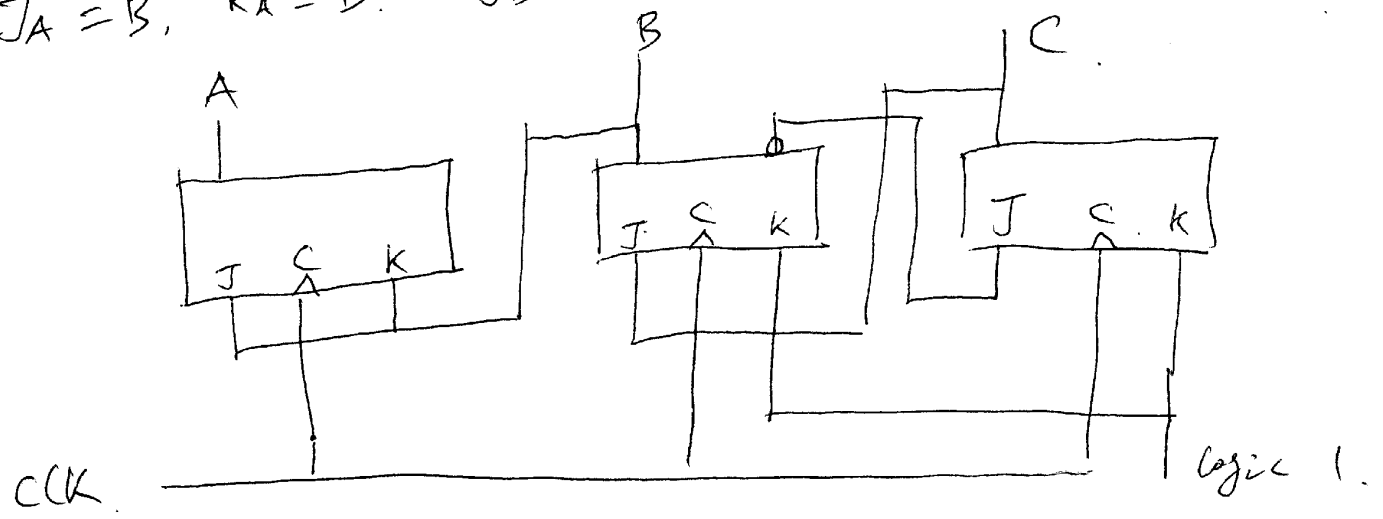
As shown above, a BCD counter can be obtained from a binary counter with parallel load. It is also possible to design a BCD counter using individual flip-flops and gates. P. 273 & 274.

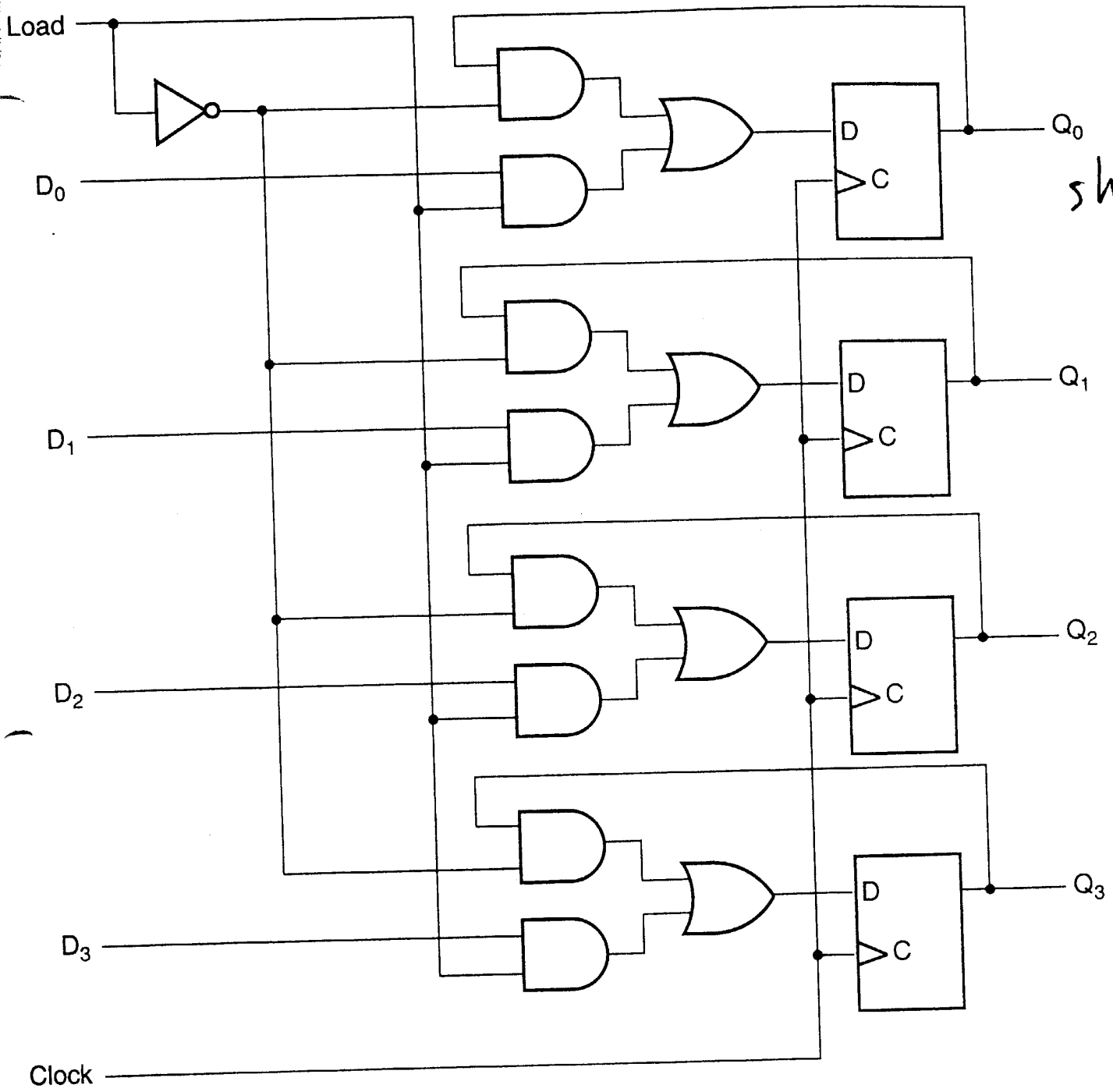
Arbitrary Count Sequence



Present state			Next state			Flip-flop inputs					
A	B	C	A	B	C	J _A	K _A	J _B	K _B	J _C	K _C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	1	0	0	x	x	1	0	x	x
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	1	1	0	x	0	1	x	x	1
1	1	0	0	0	0	x	1	x	1	0	x

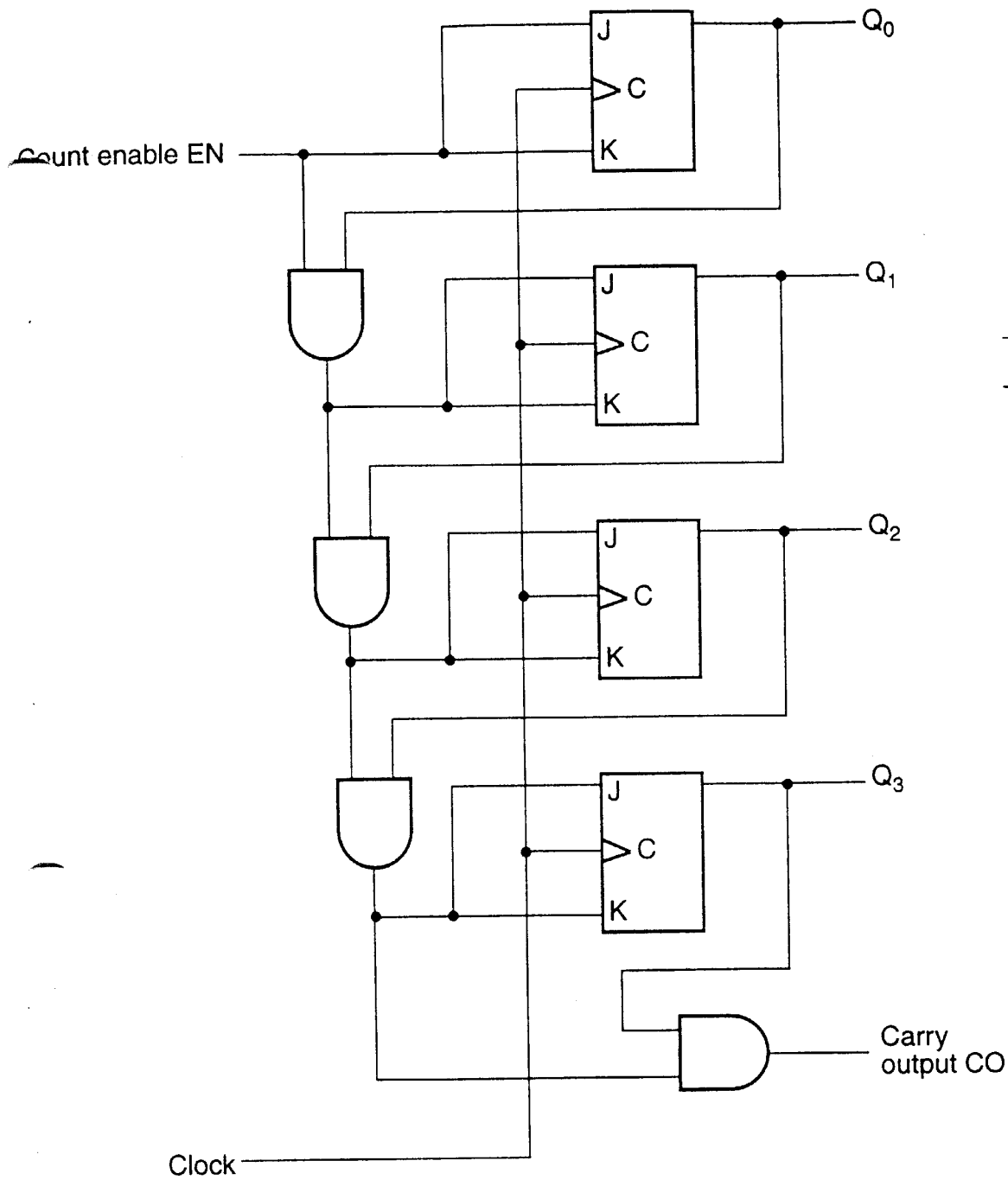
$J_A = B, K_A = B, J_B = C, K_B = 1, J_C = \bar{B}, K_C = 1$



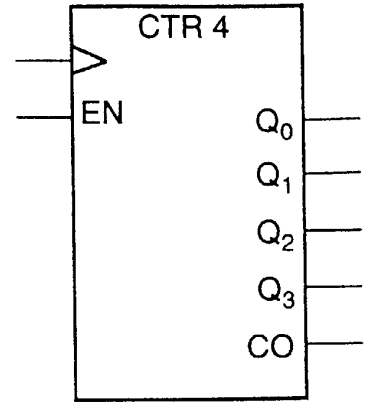


show me

□ **FIGURE 5-2**
4-Bit Register with Parallel Load



(a) Logic diagram



(b) Symbol

□ **FIGURE 5-10**
4-Bit Synchronous Binary Counter