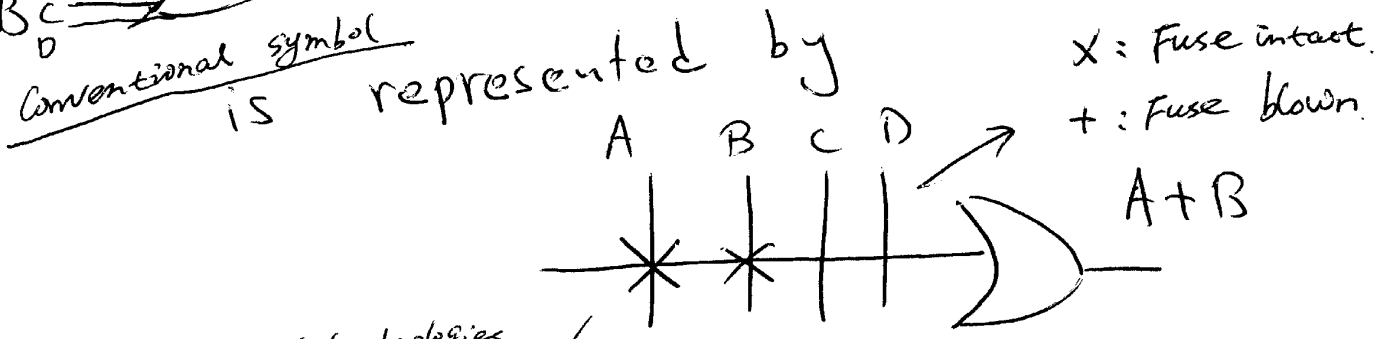
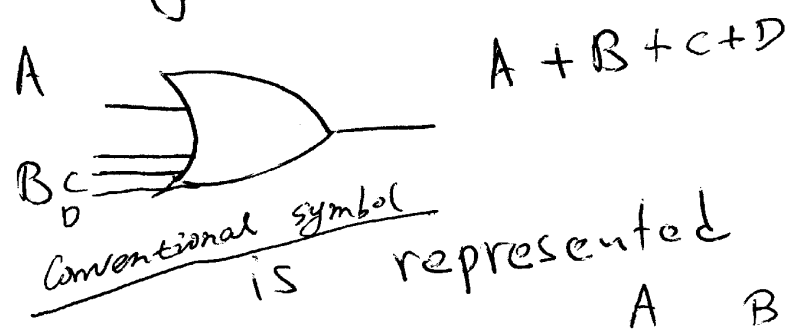


(ROM) Read Only Memory is a Programmable Logic Device (PLD).
 ↳ only allows reads.

Random Access Memory (RAM) is also a Programmable Logic Device (PLD), allowing both read(s) & write(s).

New symbols



One of the simplest technologies employs fuses.

Programming the device involves blowing those fuses along the paths that must be removed.

If an x is present at the intersection of two lines, there is a connection.
 If an x is not present, then there is no connection.

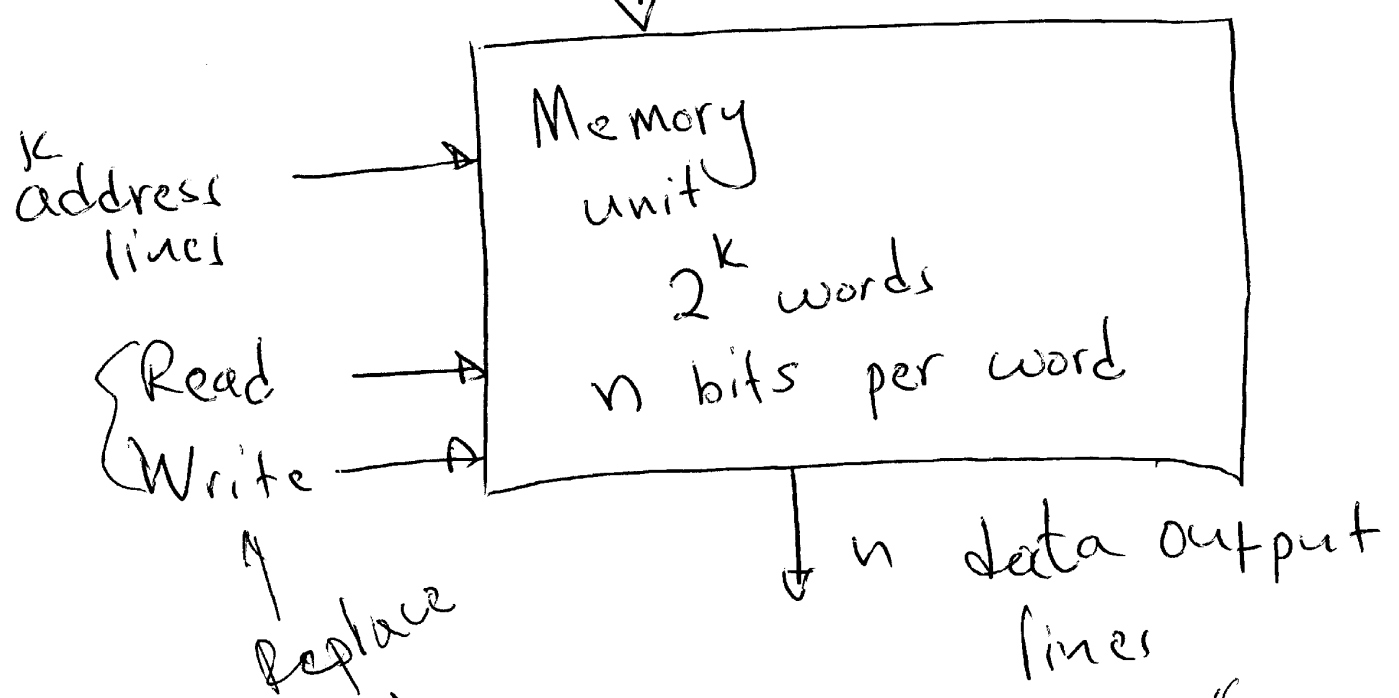
- A byte is 8 bits.
 Eg: 0000 1111 is a byte.

A word maybe 2/4 byte(s)

Eg: (ABCD)₁₆ is a 2-byte word

Memory:

n data input lines



Replace by R/W

$2^{10} = 1 \text{ Kilo}$
 $2^{20} = 1 \text{ Mega}$
 $G = 2^{30} \text{ Giga}$

$64K = 2^{16}$
 $2M = 2^{21}$
 $4G = 2^{32}$

15-3

THE PERIPHERAL COMPONENT INTERCONNECT (PCI) BUS

The PCI (**peripheral component interconnect**) bus is virtually the only bus found in the newest Pentium II systems and just about all the Pentium systems. In all of the newer systems, the ISA bus still exists, but as an interface for older 8-bit and 16-bit interface cards. Many new systems contain only two ISA bus slots. In time, the ISA bus may disappear, but it is still an important interface for many applications. The PCI bus has replaced the VESA local bus. One reason is the PCI bus has plug-and-play characteristics and the ability to function with a 64-bit data bus. A PCI interface contains a series of registers, located in a small memory device on the PCI interface, that contain information about the board. This same memory can provide plug-and-play characteristics to the ISA bus or any other bus. The information in these registers allows the computer to automatically configure the PCI card. This feature, called **plug-and-play (PnP)**, is probably the main reason that the PCI bus has become so popular in the newest systems.

Figure 15-9 shows the system structure for the PCI bus in a personal computer system. Notice that the microprocessor bus is separate and independent of the PCI bus. The microprocessor connects to the PCI bus through an integrated circuit called a **PCI bridge**. This means that virtually any microprocessor can be interfaced to the PCI bus, as long as a PCI controller or bridge is designed for the system. In the future, all computer systems may use the same bus. Even the Apple Macintosh system is switching to the PCI bus. Certainly, IBM will produce a Power-PC system that contains the PCI bus. Apple computers currently use the PCI bus.

The PCI Bus Pin-Out

As with the other buses described in this chapter, the PCI bus contains all of the system control signals. Unlike the other buses, the PCI bus functions with either a 32-bit or a 64-bit data bus and

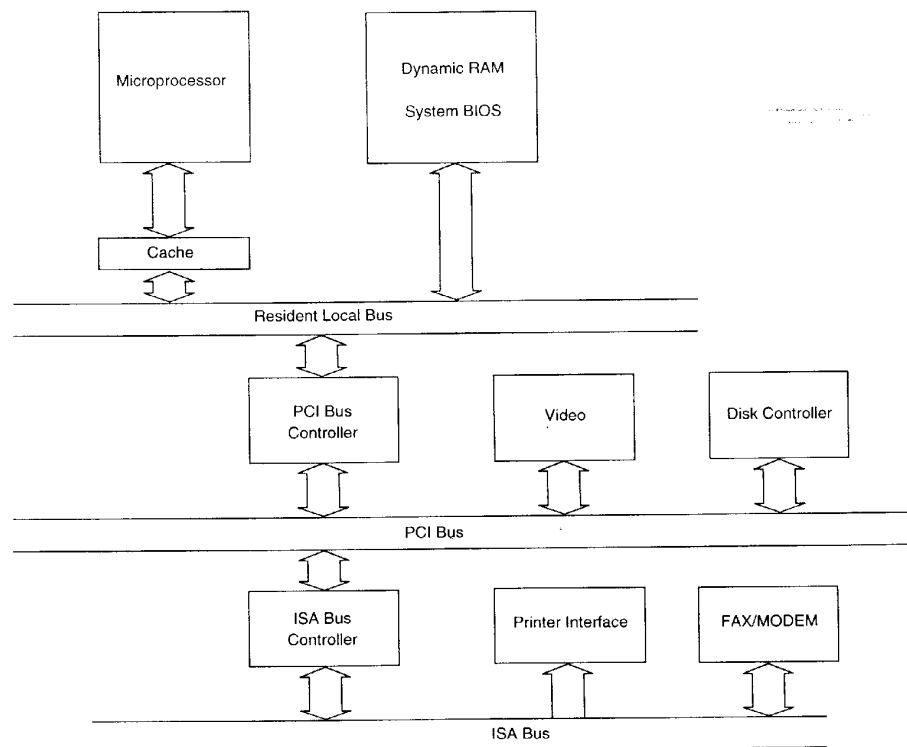
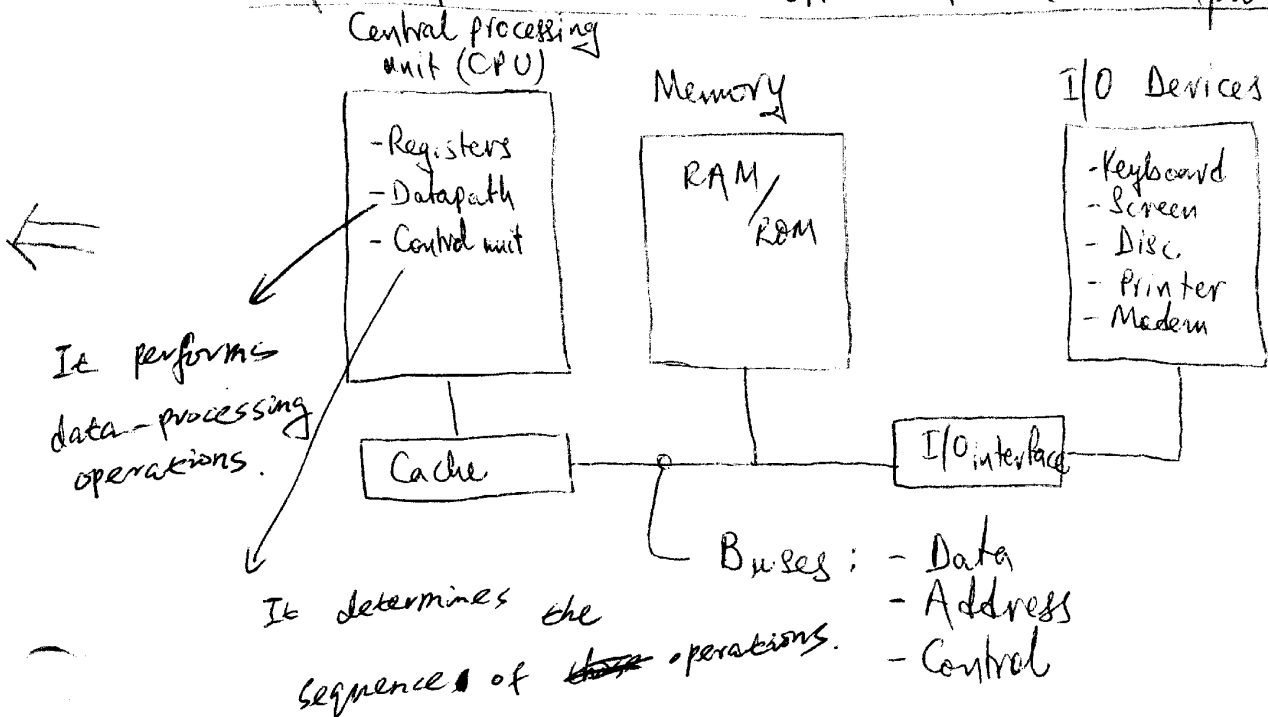


FIGURE 15-9 The system block diagram for the personal computer that contains a PCI bus.

Table 6-1:

Chip Select CS Memory Enable	Read / Write R / \bar{W}	Memory Operation
0	X	None
1	0	Write
1	1	Read

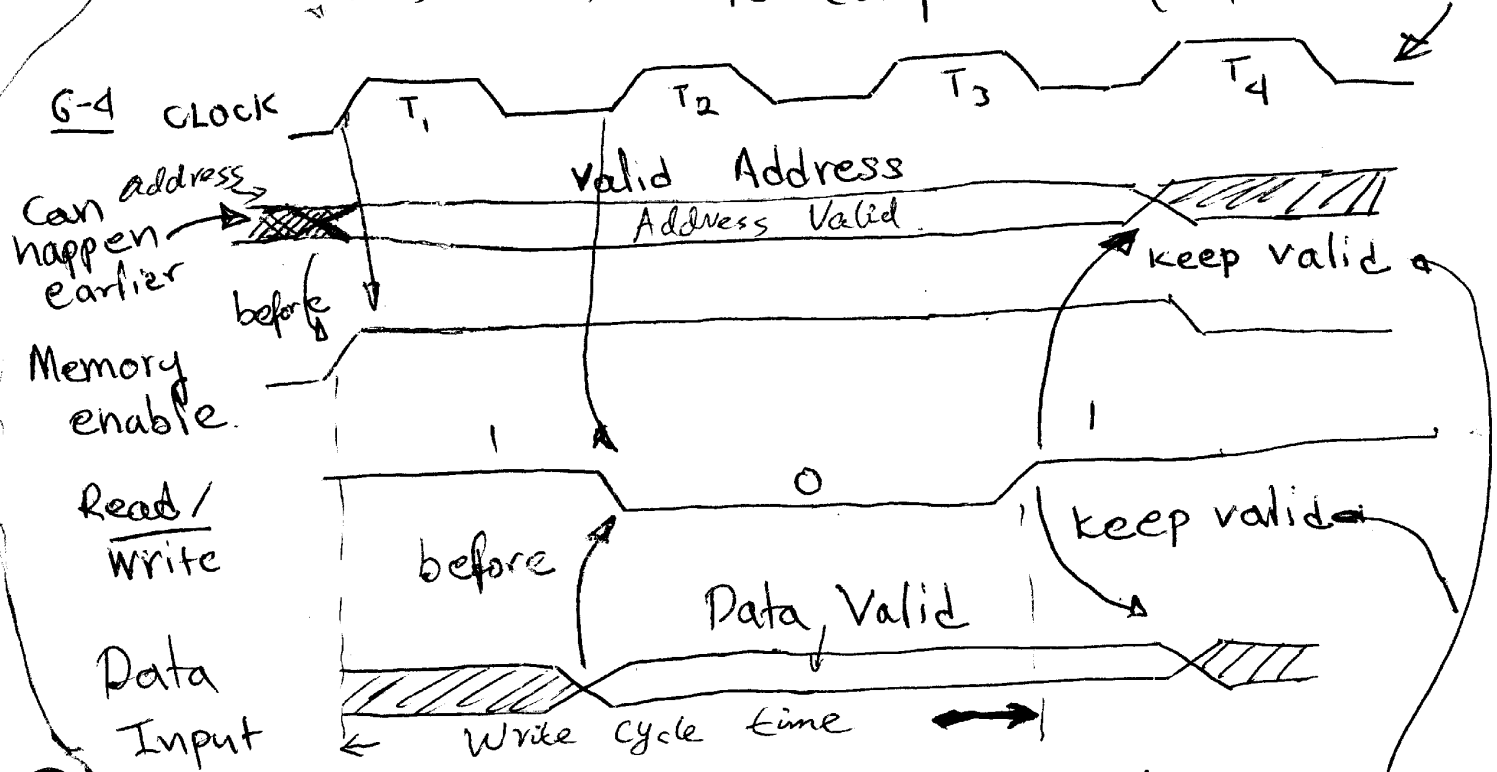
A simplified schematic of a computer system



Write Operation (simplified)

1. CPU: Apply address to address lines (+ve edge of T_1)
2. CPU: Enable the Memory (+ve edge of T_1)
3. CPU: Apply data to input lines (+ve edge of T_2)
4. CPU: Activate Write input. (+ve edge of T_2)
5. CPU: Hold data & address for memory so that it has time to process them.

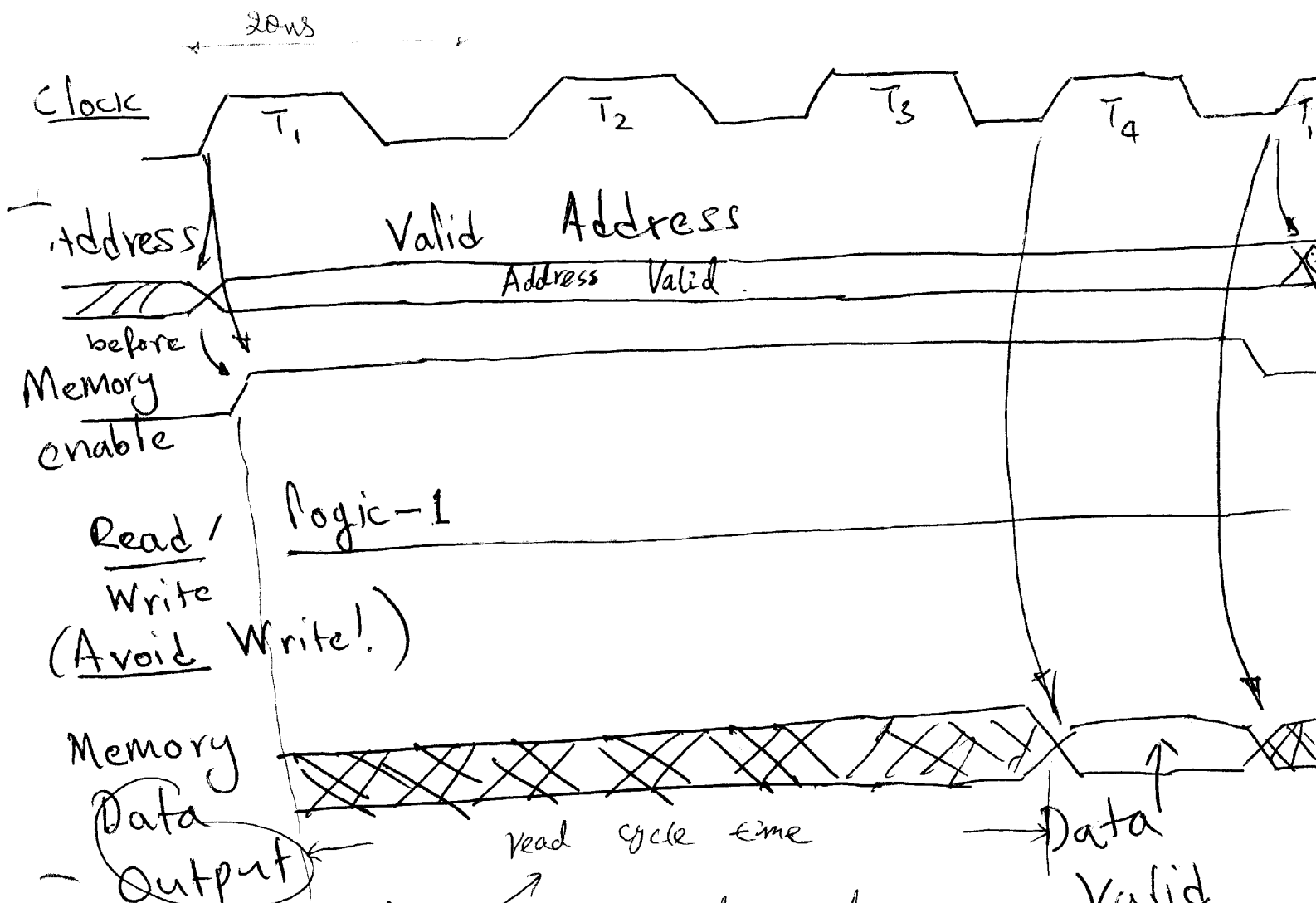
Write cycle time: maximum time taken from step 2, till memory write is complete. ($= 75 \mu s < 4 \times 20$)



From the application of the address to the completion of all memory operations to store a word. to avoid accessing & writing invalid data/address.

Read Operation

- 1. CPU: Apply the binary address.
- 2. CPU: Activate memory (enable).
- 3. CPU: Activate Read
- 4. Memory: Output data on output lines.
- 5. CPU: Read Data from data lines
- 6. CPU: Disable Memory.



Access time of a memory read operation is the maximum time from the application of the address to the appearance of the data at the data output.