

2-8 Integrated Circuits

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7

SSI: small-scale integrated devices contain independent gates (about 10).

MSI: medium-scale integrated devices contain 10-100 gates ~~is~~ performing small functions (chs 3-5)

LSI: Large-scale ~~are~~ devices for 100-few 1000s gates for small memories and programmable modules.

VLSI: Very large scale integrated circuits 1000s to 100×10^6 gates, latest μ processors.

Digital Logic Families (p 77)

TTL Transistor-transistor Logic (declining use)

ECL Emitter-coupled logic (high speed)

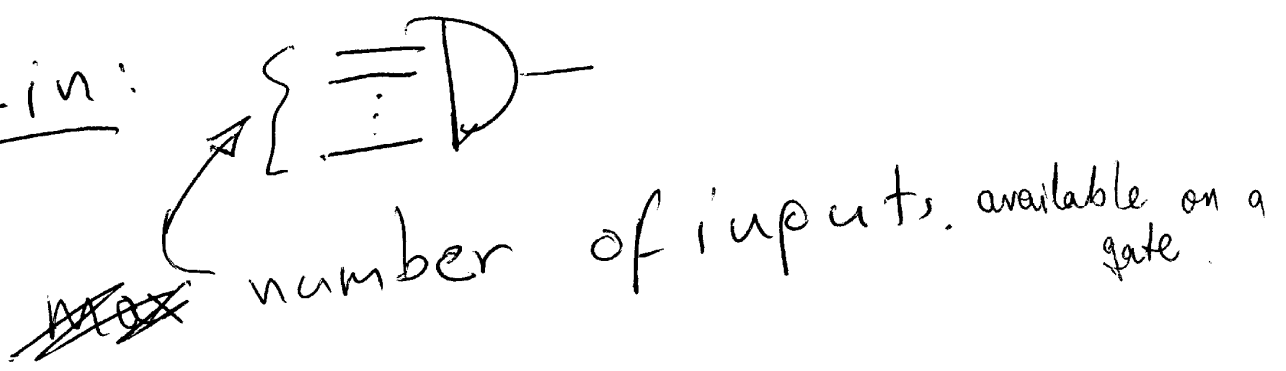
CMOS \rightarrow Complementary metal-oxide semiconductor overtaking ECL

BiCMOS \rightarrow Bipolar Complementary metal-oxide semiconductor for enhancing CMOS for providing more current

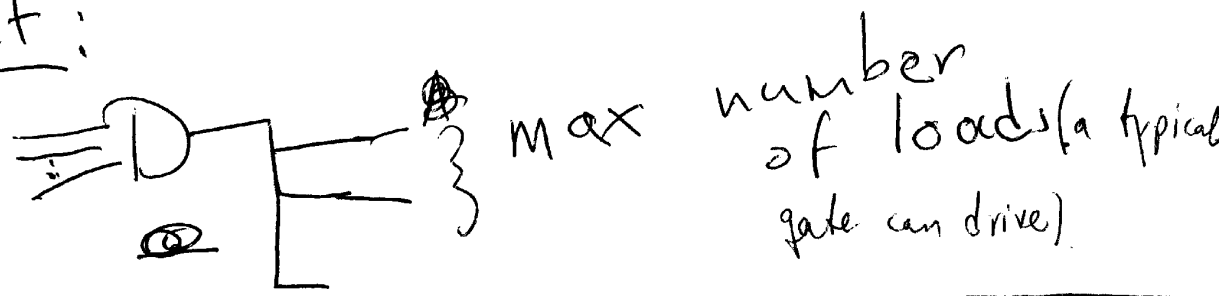
GoAs \rightarrow Very high speed.

Parameters:

Fan-in:



Fan-out:

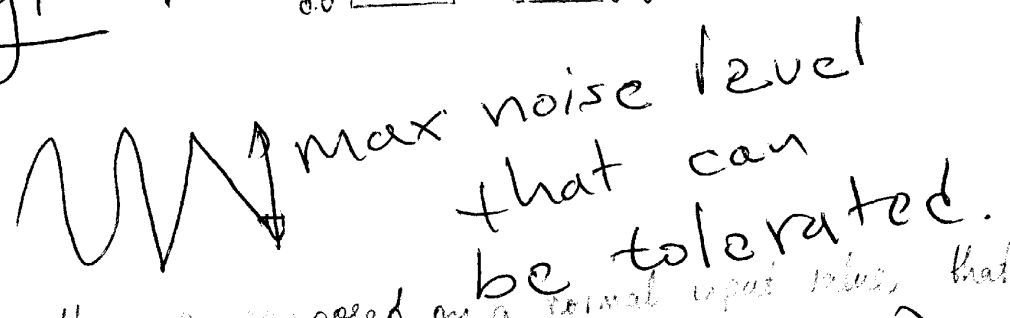


Voltage levels:

OUTPUT		INPUT	
5.0	HIGH	5.0	HIGH
4.0		3.0	
1.0	LOW	2.0	LOW
0.0		0.0	

An example of voltage ranges for binary signals.

Noise margin:



Power dissipation (related to operating @)
 on the voltage superimposed on a normal input value, that will

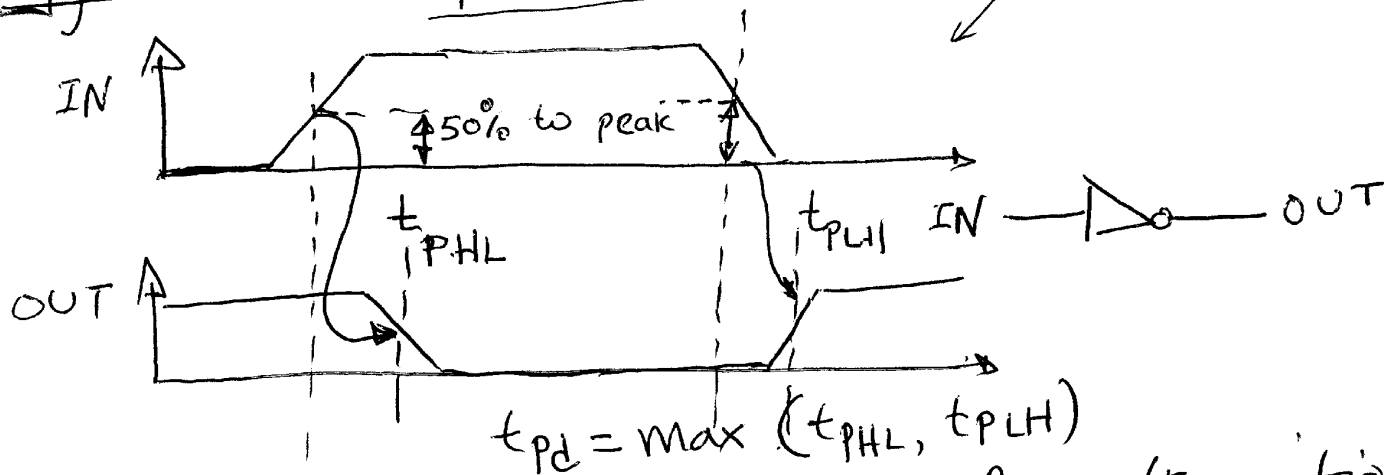
Power dissipated by the gate from the power supply.

Propagation delay

not cause an undesirable change in the circuit output.

Fig 2-40

Propagation Delay for an Inverter.



t_{PHL} = propagation time for transition from High output to low output, after change in input.

t_{PLH} = propagation time for transition from Low output to high output after change in input.

t_{pd} = propagation delay for worst case (maximum of t_{PHL} , t_{PLH})

Two different models are employed in modeling gates during simulation; 7

Transport Delay (TD) Model = delay due to propagation delay only.

Change in an output in response to the change of an input.
~~It is the time~~

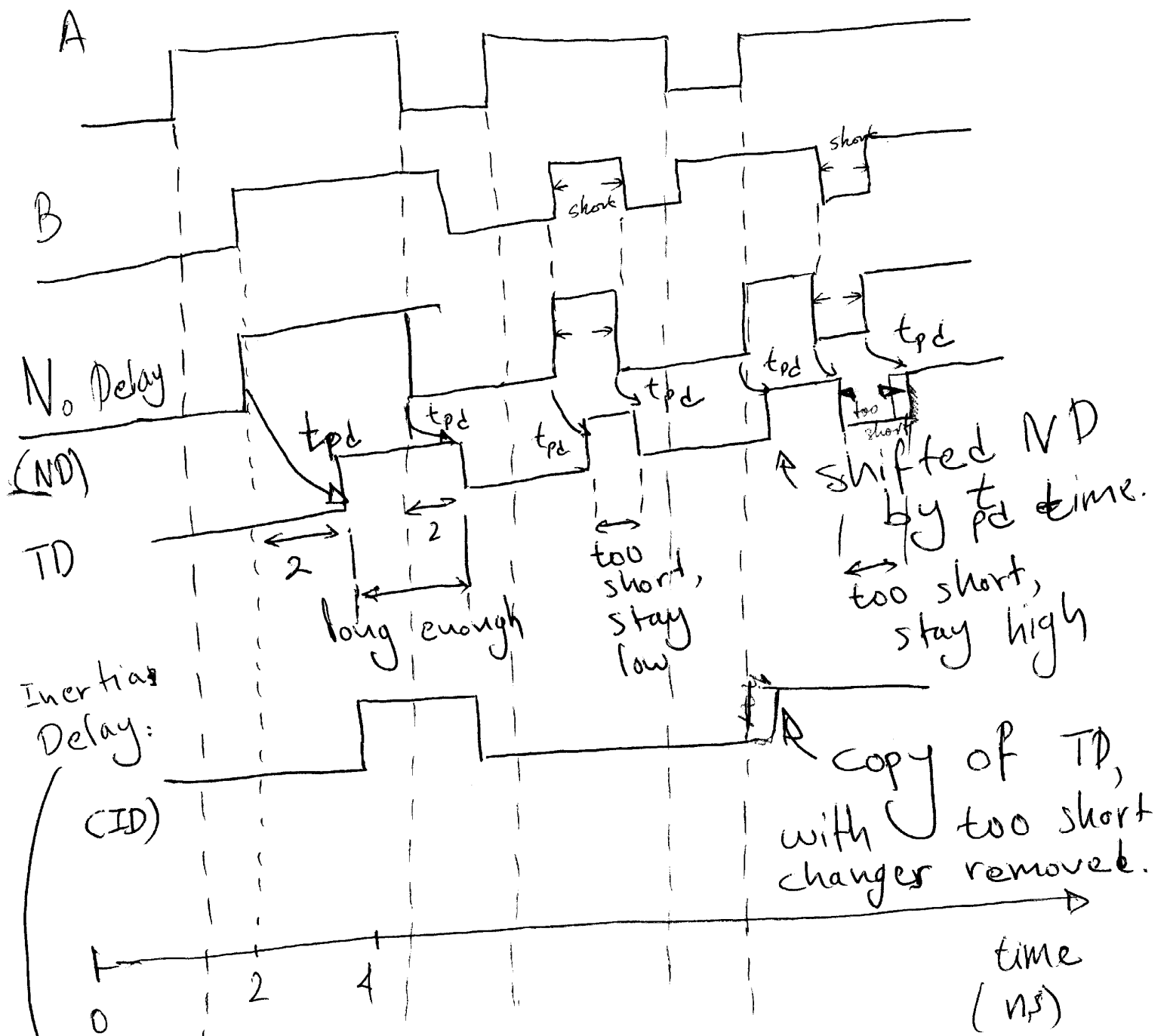
Inertial Delay (ID) Model = delay due to propagation ~~and~~

as long as the input change lasts more than the rejection time, else input change is ignored.

The rejection time is a specified value no longer than the time delay and is often equal to the time delay.

Fig 2-41

AND-gate



For every change, check that it will last more than the rejection time, else ignore:

Fig. 2-41 in book, wake A, 10-12 ns low.

Positive / Negative Logic

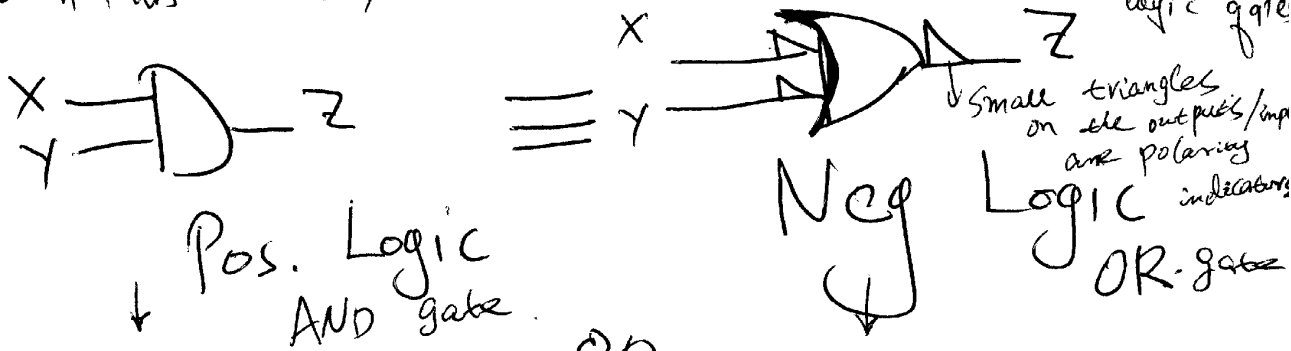
<u>signal value</u>	<u>Logic</u>	} Positive Logic
H	1	
L	0	

<u>signal value</u>	<u>Logic</u>	} Negative Logic.
H	0	
L	1	

Gates' specs are given in L/H notation

⇒ Depending on whether we adopt Positive ~~or~~ or Negative Logic, the gates mean diff things.

In this course, and in the textbook we work with positive-logic gates



X	Y	Z
0 (L)	0 (L)	0 (L)
0 (L)	1 (H)	0 (L)
1 (H)	0 (L)	0 (L)
1 (H)	1 (H)	1 (H)

P80

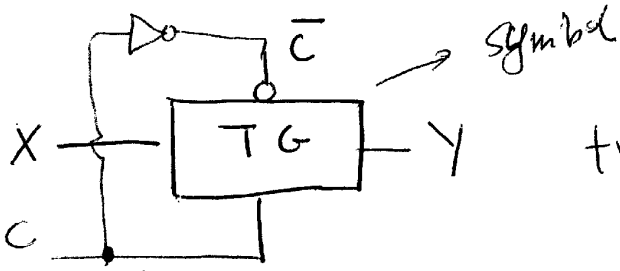
	X	Y	Z
1	1	1	1
1	0	1	1
0	1	0	0
0	0	0	0

X	Y	Z
0 (H)	0 (H)	0 (H)
0 (H)	1 (L)	0 (H) (L)
1 (L)	0 (H)	0 (H) (L)
1 (L)	1 (L)	1 (L)

Transmission Gate

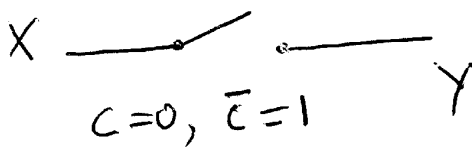
An electronic switch for connecting and disconnecting two points in a circuit.

\bar{C} & C are the control inputs and X and Y are the signals to be connected or disconnected by the TG.



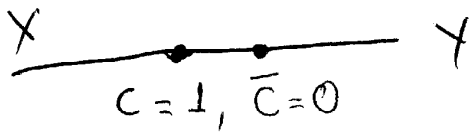
transmits X to Y if $C=1$.

In normal use, the control inputs are connected by an inverter so that C & \bar{C} are the complements of each other.



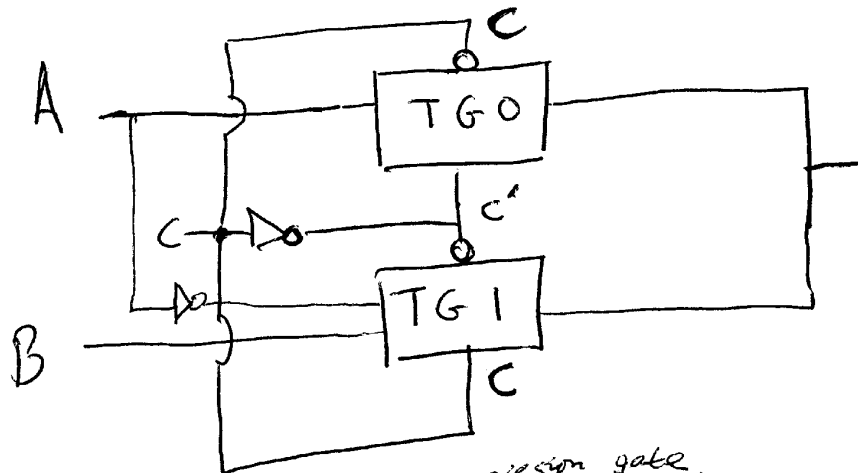
No Path

X and Y are disconnected and signals cannot pass between X and Y .



Path

X and Y are connected and signals can pass from X to Y or from Y to X .



A	C	TG1	TG0	F
0	0	No path	path	0
0	1	path	no path	1
1	0	No path	path	1
1	1	path	no path	0

To illustrate use of a transmission gate, an exclusive-OR gate constructed from two transmission gates and two inverters is shown above.

$C=1$: TG0 is "off", TG1 is "on", } $\Rightarrow F=B$

$C=0$: TG0 is "on", TG1 is "off", } $\Rightarrow F=A$