

ECE 238 - Quiz 1

Name:.....

Section:.....

Date:.....

1. Unlike languages such as C or low-level assembly which all run sequentially one instruction at a time, VHDL can be used to describe concurrent events.

- a) True b) False c) Neither

2. VHDL is case sensitive.

- a) True b) False c) Neither

3. The entity section is used to declare the _____ of the circuit.

- a) Functions
- b) Inputs and outputs
- c) Behavior
- d) Components

4. The SIGNAL statement can be thought of as a _____ inside the device.

- a) Port
- b) Component
- c) Physical wire
- d) Entity

5. The architecture section is used to declare the _____ of the circuit.

- a) Functions
- b) Inputs and outputs
- c) Behavior
- d) Components

6. Consider the following code:

```

4  entity circuit1 is
5  port (
6      a: in std_logic;
7      b: in std_logic;
8      c: in std_logic;
9      d: in std_logic;
10     y: out std_logic;
11     x: out std_logic
12 );
13
14 architecture circuit1_behavior of circuit1 is
15     signal sig1: std_logic;
16     signal sig2: std_logic;
17
18     begin
19         sig1 <= not(a) and b;
20         sig2 <= c xor d;
21         y <= sig1 or sig2;
22         x <= sig2 and a;
23     end circuit1_behavior;

```

6.1 Draw its corresponding logic diagram.

6.2 As a hardware description language, the code in lines 19-22 follows a sequential order (i.e., event order follows a textual order).

- a) True b) False c) Neither

6.3 Assume that there is a change on the value of the input signal **c**. Thus,

- a) All the statements (line 19 to line 22) are *concurrently executed*.
b) All the statements are *sequentially executed*.
c) All the statements except line 20 are *concurrently executed*.
d) The above options are not correct.

7. In VHDL, we can write a concurrent statement as:

```
a <= not(a);
```

7.1 Draw the logic diagram for the above VHDL statement.

7.2 Describe the operation of the circuit in part 7.1