

# ECE238 - Lab 3

Name:.....  
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Section:.....

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## Part 1

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A half adder is an arithmetic circuit that generates the sum of two binary digits. The circuit has two inputs, X and Y, and two outputs, S and C. The input variables are the augend and addend bits to be added, and the output variables produce the sum (S) and the carry (C). Write a VHDL description for a half adder using concurrent signal assignments only. For doing so, simplify the boolean expressions for the output lines in terms of the inputs and use the expressions directly in the assignment statements. Figure 1 shows the true table for the half adder.

Inputs		Outputs	
X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Figure 1. Truth table of half adder.

Test the half-adder for all possible combinations of inputs. Turn in the VHDL code, the testbench and the waveforms.

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## Part 2

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A full adder takes two inputs, X and Y, and a carry-in (Z), and generates the sum (S) and carry-out (C). Figure 2 shows the true table of the full adder.

Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 2. Truth table of the full adder.

Write a VHDL description for a full-adder using only half adders previously designed and an OR gate, as showed in Figure 3.

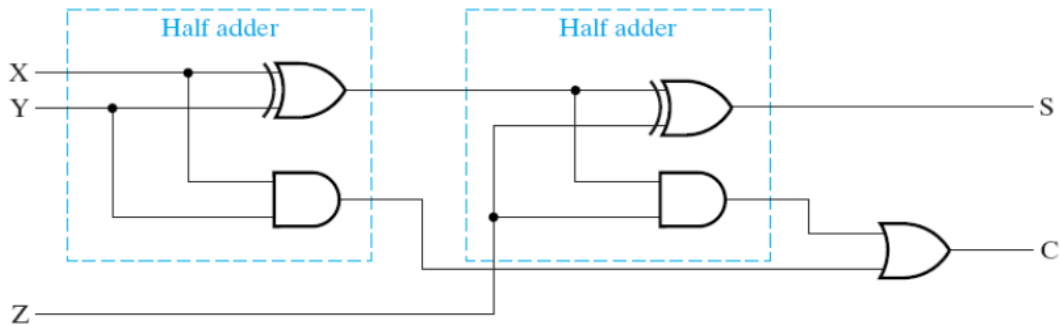


Figure 3. Full adder circuit built by using half adders and an OR gate.

Test the full-adder for all possible combinations of inputs. Turn in the VHDL code, the testbench and the waveforms.