

# ECE238 - Lab 6

Name:.....  
Date:.....  
Section:.....

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## Part 1

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The specifications for the sequence detector you have to design are given as follows. The system accepts a serial input **X** as well as inputs **CLK** and **RESET**, and has as a five-bit output **Z**. It has to be synchronized with the rising edge of the signal **CLK**. The **RESET** signal is used to reset the sequence detector to the initial state, where the output **Z** = 00000. The serial sequence to be detected is "00101", and the output **Z** is specified as:

- Z**=00000; when no sequence is detected; i.e., initial state.
- Z**=00001; when the first bit of the sequence is detected.
- Z**=00010; when the second bit is detected.
- Z**=00100; when the third bit is detected.
- Z**=01000; when the fourth bit is detected.
- Z**=10000; when the whole sequence is detected.

Derive the state machine of the sequence detector. Then, write the corresponding VHDL code, simulate and implement on the FPGA. For the simulation part, test the state machine with the input sequence **X** = "0011000101001011". For the implementation part, connect the output **Z** to the discrete LEDs.

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## Part 2

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Write two VHDL descriptions, sm1.vhd (Figure 1) and sm2.vhd (Figure 2), for the state machines showed below. Both state machines accept as inputs **X**, **RESET** and **CLK**, and have as output a bit **OUTPUT**. Test the state machine 1 with the input sequence **X** = "01001100110", and the state machine 2 with the input sequence **X** = "0001000100110". Turn in sm1.vhd, sm2.vhd and the two waveforms for the above mentioned test cases. **You need not implement on the FPGA.**

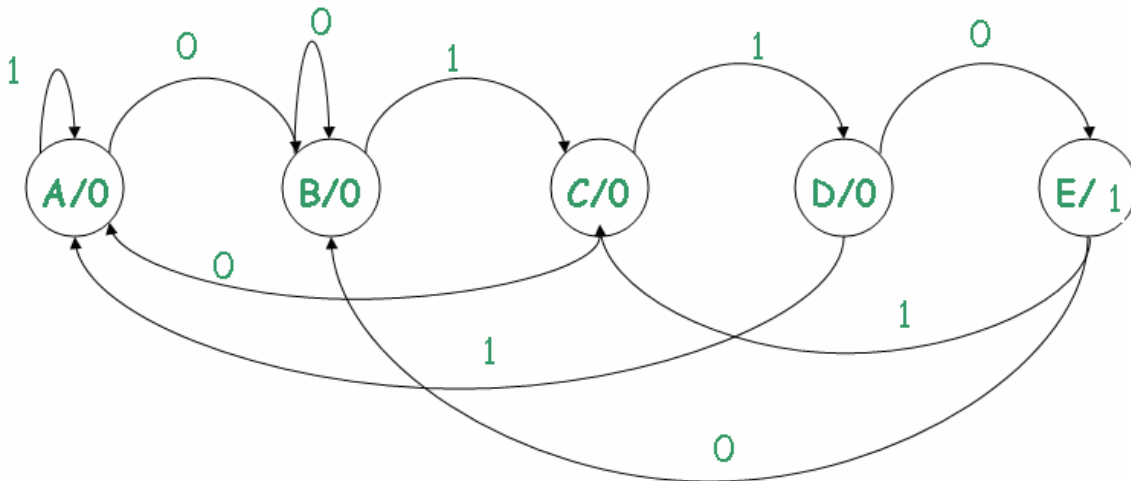


Figure 1. State machine 1.

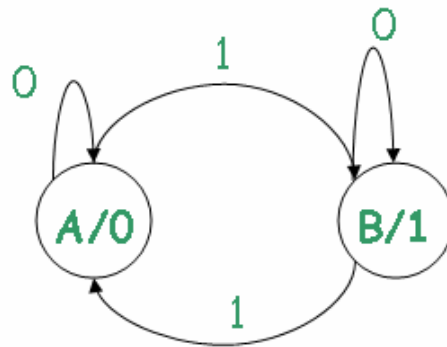


Figure 2. State machine 2.

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### Part 3

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Write a VHDL description, `sys.vhd`, for the system showed in Figure 3. State machine 1 and 2 refer to the state machines implemented in **Part 2**. The system accepts the inputs **X**, **CLK** and **RESET**, and has as output a bit **OUTPUT**. Simulate your system with the input **X** = "010011001101100000110". Turn in `sys.vhd` and the waveform for the above mentioned test case. In addition, implement on the FPGA board. **You need not implement on the FPGA.**

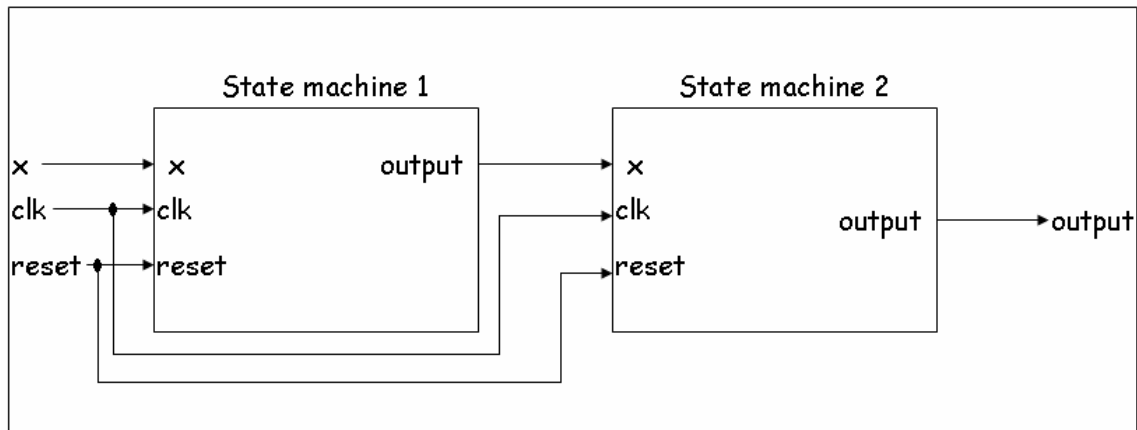


Figure 3.