

ECE 238 – Lab 6

Finite/Algorithmic State Machines (FSM/ASM)

Name.....

Section.....

Part 1

In digital communications, a special synchronization pattern, known as *preamble*, is used to indicate the beginning of a packet. For example, the Ethernet II preamble includes eight repeating octets of “10101010”. We wish to design an FSM that generates the “10101010” pattern. The circuit has an input signal, **start**, and an output, **data_out**. When start is ‘1’, the “10101010” pattern will be generated in the next eight clock cycles [1].

- a) Derive the state diagram.
- b) Convert the state diagram to an ASM chart.
- c) Derive the VHDL code according to the ASM chart.
- d) Simulate the system.

Part 2

Now we wish to design an FSM to detect the “10101010” pattern in the receiving end. The circuit has an input, **data_in**, and an output signal, **match**. The match signal will be asserted as “1” for one clock period when the input pattern “10101010” is detected [1].

- a) Derive the state diagram.
- b) Convert the state diagram to an ASM chart.
- c) Derive the VHDL code according to the ASM chart.
- d) Simulate system.

References

[1] P. Chu, *RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability*, Wiley, 2006, pp. 369 - 370.