Lab 7 – State Machines
Due TODAY!

Name: ……..
Section:…….
Date:…….

Write a VHDL description for the ASM shown in Fig. 1. The one-bit inputs are given by **a** and **b**, and the one-bit outputs by **y0**, **y1** and **y2**. Note that in the ASM diagram an output signal (**y0**, **y1** or **y2**) is assumed to take the default value '0' (not don't-care) if it is not listed inside the state box (Moore output) or inside the conditional output box (Mealy output). For example, the output **y0** is only asserted (logic '1') at state S0; otherwise it takes a value '0'. Attach 1- the VHDL code for the system; 2- the testbench and waveform. In the waveform file, *clearly* show when and why output signals are asserted.

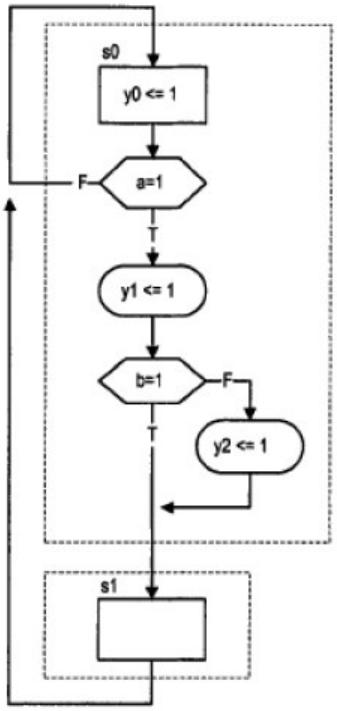

Figure 1.