

ECE 238 - Lab 9

Repetitive-subtraction division

1 Introduction

Repetitive-subtraction division is an algorithm to implement division operation. Let y and d be the dividend and divisor respectively. This algorithm obtains the quotient q and the remainder r by subtracting d from y repeatedly until the remaining of y is smaller than d . Assume that all signals are 8 bits wide and interpreted as unsigned integers.

In this lab, you are asked to implement the repetitive-subtraction division algorithm that, given y and d , returns q and r .

The input signals are:

- *start*: the circuit starts operation when the start signal is activated.
- *y*: dividend, a 8-bit number.
- *d*: divisor, 8-bit number.
- *clk*: system clock.
- *reset*: asynchronous reset signal.

The output signals are:

- *q*: quotient, a 8-bit number.
- *r*: remainder, a 8-bit number.
- *ready*: status signal. It is asserted when the circuit is idle and ready to accept new inputs. It can also be interpreted that the previous operation has been completed.

2 Lab Task

- Derive the pseudo-code for the repetitive-subtraction;
- Derive the ASM for the pseudo-code of item (i);
- Derive the VHDL code;
- Simulate the system;
- Turn in all above items.