ECE 238 - Final Project
Fibonacci Function
Work on this project individually!

1 Introduction

Consider the following sequence of numbers:

$$0, 1, 1, 2, 3, 5, 8, 13, 21, 34, ..., \tag{1}$$

By carefully inspecting the above sequence, we can note that each number is the sum of its two immediate predecessors. More formally, a *Fibonacci* number F_n is generated by the simple rule:

$$F_n = \begin{cases} 0 & \text{if } n = 0 \\ 1 & \text{if } n = 1 \\ F_{n-1} + F_{n-2} & \text{otherwise} \end{cases}$$

In this lab, you are asked to implement in hardware a Fibonacci function that, given a number n, returns the Fibonacci number F_n.

The input signals are:

- n: a 5-bit input number.
- *start*: the circuit starts operation when the start *signal* is activated.
- *clk*: system clock.
- *reset*: asynchronous reset signal.

The output signals are:

- F: the Fibonacci number F_n.
- *ready*: status signal. It is asserted when the circuit is idle and ready to accept new inputs. It can also be interpreted that the previous operation has been completed.

2 Lab Task

1. Derive the in pseudo-code to compute the Fibonacci number F_n.
2. Derive ASM of for the pseudo-code of item 1.
3. Derive the VHDL code.
4. Simulate the system.
5. Attach a brief report explaining your design. Provide a section for 1- introduction; 2- the pseudo-code; 3- the ASM; 4- the VHDL code; 5- the simulation results; 6- conclusion.

References

[1] P. Chu, RTL Hardware Design Using VHDL, Chapter 11, pp. 373-420, 2006.