

ECE 238 - Final Project
A leading-zero counting circuit
Work in this project individually!

1 Introduction

A leading-zero counting circuit counts the number of consecutive 0's from an input signal. We want to design a sequential version of this circuit. The design should check one bit of the input at a time and increment accordingly. The counting stops when the first 1 is encountered. In this lab, you are asked to implement the leading-zero counting circuit.

The input signals are:

- *n*: a 16-bit input number. We want to count the leading 0's of *n* (starting at the most significant bit).
- *start*: the circuit starts operation when the start *signal* is activated.
- *clk*: system clock.
- *reset*: asynchronous reset signal.

The output signals are:

- *count*: the number of leading zeros.
- *ready*: status signal. It is asserted when the circuit is idle and ready to accept new inputs. It can also be interpreted that the previous operation has been completed.

2 Lab Task

1. Derive the in pseudo-code to compute the number of leading zeros.
2. Derive the ASM for the pseudo-code of item 1.
3. Derive the VHDL code.
4. Simulate the system.

5. Attach a brief report explaining your design. Provide a section for 1- introduction; 2- the pseudo-code; 3- the ASM; 4- the VHDL code; 5- the simulation results; 6- conclusion.

References

- [1] P. Chu, RTL Hardware Design Using VHDL, Chapter 11, pp. 373-420, 2006.