LAB Assignment #2 for ECE 337

Assigned: Mon., Oct. 24, 2011
Due: Wed., Oct. 26, 2011

Description: Download VHDL files for UART and ASCII2BIN, create an ISE project and program the FPGA.

This assignment is designed to give you exposure to the programming an FPGA. You need to create a project and add ALL of the supplied files to it, INCLUDING THE UARTNumberConvert.ucf file. Generate a bit file by running the ISE synthesis flow. Program the FPGA using the Adept software tool, e.g., select the 'projectname.bit' file which is created in the ISE project directory, where 'project name' is the name you used when you created the ISE project. The Adept tool will complain with the message: 'Startup clock for this file is 'CCLK instead of 'JTAB CLK', which you can safely ignore.

You need to install 'putty' (or a suitable substitute) that will allow you to connect to the serial port. With putty, choose the 'Serial' radio button and be sure to set the serial line to the proper serial port (use Control panel/Device Manager/Ports(COM & LPT) to determine which port is active using the TrendNet USB adapter). Also be sure to set the baud rate to 9600 if this is not the default. Other important parameters (which are the default in putty) are 8 data bits, N (no parity), 1 stop bit and NO flow control.

Once putty is running and the FPGA is programmed, you can test the VHDL code as follows:

- Type up to a 4 digit number in the range of -1024 and 1023, press <enter>
- Type a second 4 digit number (same range), press <enter>
- Push BTN1 on the FPGA. The sum of these two numbers should appear in the putty terminal.
- Repeat this operation for other pairs of numbers.

NOTE: You will NOT see the two numbers that you type (unless you have local echo turned on). Pressing BTN0 performs a reset of the FPGA board.

Laboratory Requirements:

1) In class DEMO on the due date.

Grading:
100 pts will be given for a proper demonstration.