# LAB Assignment #3 for CMPE 415

Assigned: Fri., Oct 19, 2007
Due: Thur., Nov 8th, 2007

Description: Write a LABVIEW code to reproduce the testbench waveforms from LAB #2 and demonstrate a serial data transfer with the FPGA.

The state machine that you coded for the FPGA in LAB #2 serves as the receiver task in the serial transfer process. We will use LABVIEW to implement the sender task. In the tutorial, we covered more advanced features of LABVIEW and developed several VIs that function to read and write one bit to the parallel port data and status registers. We also began to work on the parent VI that implements the testbench. I indicated in class that the code that I showed you was still under development. I'll warn you in advance that I needed to make changes to the code that I showed you in order to get it to work.

Some of those changes involved using different pins on parallel port registers. For example, I originally used the Control register bit 0 for the clock, but since then have dropped the use of the Control register altogether. The front panel of my VI is shown below. Note that I use only the Data
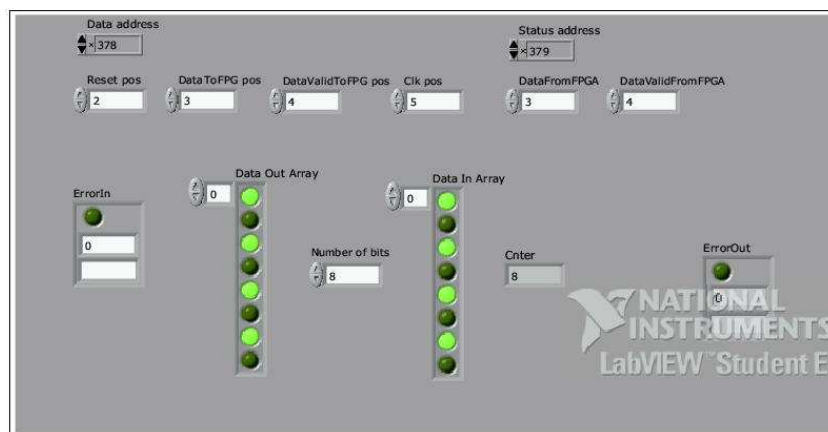
and Status registers of the parallel port. This also required that I change the transparport.ucf and transparport.xcf files that you may have already downloaded. YOU MUST USE THE NEW VERSIONS OF THESE FILES THAT ARE NOW ON-LINE.

In order to help you succeed with this project, I've also posted my verilog code for those who could not get theirs to work properly. A flow chart that indicates the sequence of events that need to occur in the LABVIEW code is given in the figure.

Laboratory Report Requirements:

1) Turn in a commented copy of your LABVIEW code.
3) Prepare to demonstrate that both the LABVIEW code and the FPGA can communicate properly.

Each of you MUST work on it **independently** and turn in a separate report, i.e., this is NOT a group project.

```
┌─────────────────┐     ┌─────────────────┐     ┌──────────────────────┐
│  ClkToFPGA = 0  │ ──▶ │ Pulse Reset high│ ──▶ │ DataValidToFPGA = 1  │──┐
└─────────────────┘     └─────────────────┘     └──────────────────────┘  │
                                                                           │
   ┌───────────────────────────────────────────────────────────────────────┘
   │
   │   ┌─────────────────────────────┐     ┌──────────────────┐
   └─▶ │ Write bit to DataToFPGA port│ ──▶ │ Pulse ClkToFPGA  │──┐
   ▲   └─────────────────────────────┘     └──────────────────┘  │
   │                                                              │
   │            no        ◇ Cnt == 8 ◇ ◀──────────────────────────┘
   └──────────────────────◇         ◇
                               │ yes
                               ▼
                    ┌──────────────────────┐
                    │  DataValidToFPGA = 0 │                        bit == 0
                    └──────────────────────┘
                               │
                               ▼
         ┌───────────────────────────────────────────┐      ◇
   ┌───▶ │ Read bit from DataValidFromFPGA port       │ ──▶ ◇ ◇
   │     └───────────────────────────────────────────┘      ◇       bit == 1
   │                                                         
   │     ┌──────────────────┐   ┌────────────────────────────────────┐
   │     │ Pulse ClkToFPGA  │◀──│ Read/save bit from DataFromFPGA port│
   │     └──────────────────┘◀──│           Increment Cnt            │
   │            │               └────────────────────────────────────┘
   │   no       ▼        yes    ┌────────┐
   └──────◇ Cnt == 8 ◇ ──────▶  │  Done  │
          ◇         ◇           └────────┘
```
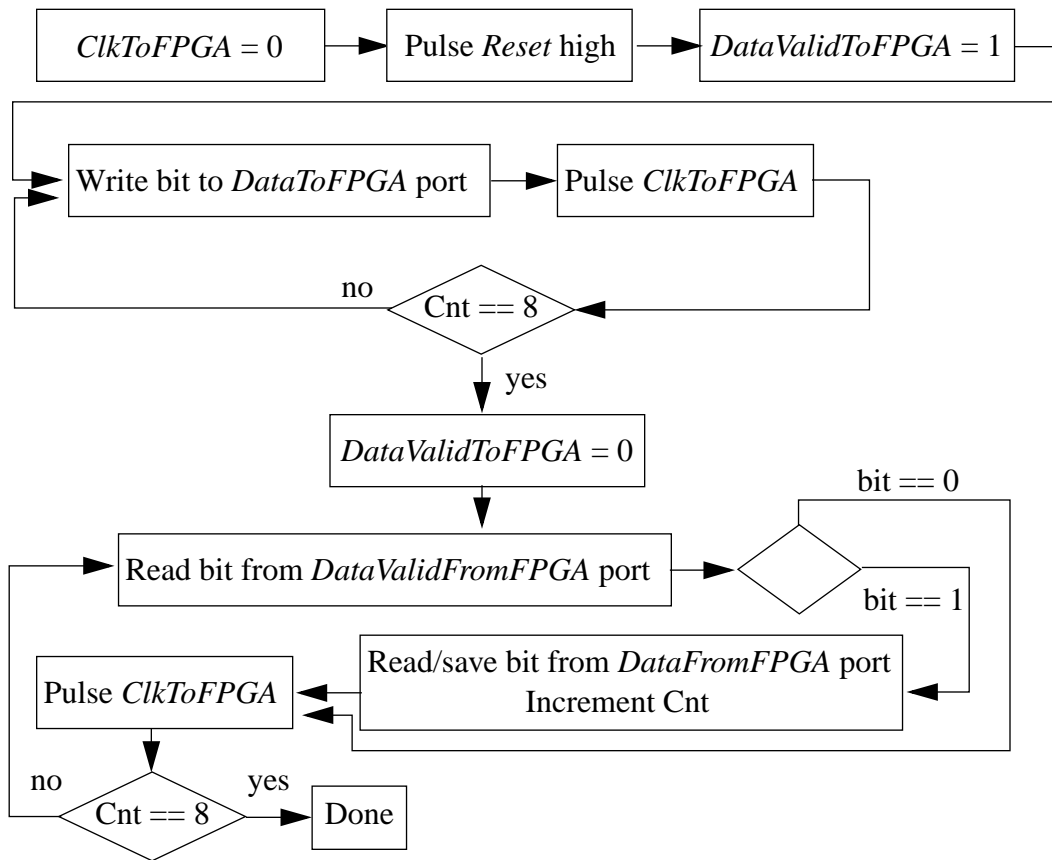
Grading:
60% LABVIEW code correctly specifies desired functionality.
10% Meaningful comments in LABVIEW code.
30% Successful hardware demonstration.