CMPE 415: Programmable Logic Devices

Course:

CMPE 415: Programmable Logic Devices, Fall 2007. 3 credits.

Course Instructor:

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Office Hours: T-Th 5:30-6:30pm or by appointment

Text:

The Design Warrior's Guide to FPGAs, Devices, Tools and Flows, Clive "Max" Maxfield, ISBN: 0-7506-7604-3

Modeling, Synthesis and Rapid Prototyping with the Verilog HDL, Michael D. Ciletti, ISBN: 0-13-977398-3

Supplementary text:

Advanced Digital Logic Design Using Verilog, State Machines and Synthesis for FPGAs, Sunggu Lee, ISBN: 0-534-55161-0

Grading:

The distribution of weights for the exams, homeworks and projects is as follows:

Exam 1	20%
Final	25%
Labs/Homeworks	25%
Projects	25%
Class Participation	5%

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

The final exam is cumulative. However, material covered after the second exam will be emphasized.

Students are encouraged to participate in class.

NOTE: Cheating at any time in this course will cause you to fail the course.

Please refer to the guidelines on the next page.
For a complete description of academic dishonesty, refer to the UMBC Student Handbook.

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The following is taken from the UMBC Student Handbook:

DEFINITIONS OF ACADEMIC MISCONDUCT

Academic misconduct may include but is not limited to the following:

Cheating: knowingly using or attempting to use unauthorized material, information, or study aids in any academic exercise.

Fabrication: Intentional and unauthorized falsification or invention of any information or citation in an academic exercise.

Facilitating Academic Dishonesty: Intentionally or knowingly helping or attempting to help another commit an act of academic dishonesty.

Plagiarism: Knowingly representing the words or ideas of another as one's own in any academic exercise, including works of art and computer-generated information/images.

POLICY FOR RESOLVING CASES OF ACADEMIC MISCONDUCT

Individual faculty members have the right and responsibility to deal directly with any cases of academic misconduct which arise in their courses. Instances of academic misconduct may be identified in one of two ways. If a faculty member believes a student has committed an act of academic misconduct--for example, by direct observation of student behavior, by comparing the contents of an assignment with that submitted by another student, or by reviewing notated sources or references--the faculty member, in consultation with the Chair of the Academic Conduct Committee, will assess the student's alleged misconduct and the faculty member's options. If a student believes that academic misconduct has occurred, the student will notify either the faculty member or the Chair of the Academic Conduct Committee.

It is particularly important that the Chair of the Academic Conduct Committee be consulted. The Chair can provide knowledge and insight for the faculty member. Communication of instances of academic misconduct also protects the integrity of the university by providing a means of recording infractions that may be repeated by a particular student, or which may prove endemic to a particular course or department. Consultation with the Chair of the Academic Conduct Committee provides a formal record of the infraction and resolution, protecting the student, professor, and university should any questions later arise.

The student will have the opportunity to respond to an accusation of academic misconduct.

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Tentative Course Outline:

Date	Topic
Week 1	Introduction
Week 2	Introduction to Verilog
	Overview of Verilog
Week 3	FPGA Architectures I
	Lab: ISE tutorial
Week 4	FPGA Architectures I
	Lab: XESS tutorial
Week 5	Verilog Data Types and Operators
	Lab: LAB #1 demos (Xilinx)
Week 6	Verilog Event Driven Simulation
	Lab: LABVIEW tutorial
Week 7	Verilog Behavioral Constructs
	Verilog State Machines
Week 8	**Lab**: LAB #2 demos (LABVIEW)
	Lab: LABVIEW tutorial (cont) & Xilinx CORE generator tutorial
Week 9	Class cancelled
	Class cencelled
Week 10	Midterm
	Midterm review
Week 11	Verilog State Machines
	Lab: LAB #3 demos (LABVIEW&Xilinx)
Week 12	FPGA Architectures II
	Lab: LAB #4 demos (LABVIEW&Xilinx) Project assigned
Week 13	FPGA Architectures II
	Verilog Design Examples
Week 14	Verilog Design Examples
	FPGA Architectures III
Week 15	FPGA vs. ASIC Design Styles
	Schematic-based and HDL-based Design Flows
Week 16	**Lab:** Project demos
	Final exam

(Note: Changes/Additions to this schedule will be posted on my web site http://www.cs.umbc.edu/~plusquel/415)