Differential Distribution

Differential clocks are more robust to noisy environments than single-ended clocks for 2 reasons:

- Signal swing is twice that of single-ended.
  Therefore, they can tolerate twice the interference
- Any *common mode noise* is cancelled out completely in the receiver.

Crosstalk problems are particularly acute in TTL systems that use an ECL clock distribution.

The low skew characteristics of an ECL system make it attractive.

However, the ECL signals **are low** in amplitude, and the larger TTL signals easily generate interfering crosstalk at the ECL receivers.

Making the ECL clock distribution differential helps overcome common mode noise problems created by this type of crosstalk.

Differential Distribution

Bear in mind that this strategy does not help with "single-sided" crosstalk, i.e., crosstalk created by one clock wire and a signal wire running too close to one another.

Differential signaling helps a lot with communications *between boards*.

The difference in the noise voltage on the GND planes of the two systems cancel in the differential receiver.

Clock Duty Cycle:

The ideal duty cycle for a clock signal is 50%.

The **falling edge** precisely bisects the signal changes in data wires.

The *average DC value* of an ideal clock lies halfway between the HI and LO states.

The property allows for the design of a simple feedback mechanism designed to keep the duty cycle fixed at 50%.

Clock Signal Duty Cycle

The **asymmetric** nature of rising/falling wfms of *clock repeaters* is the reason why clocks drift away (become unbalanced) form the 50% duty cycle.

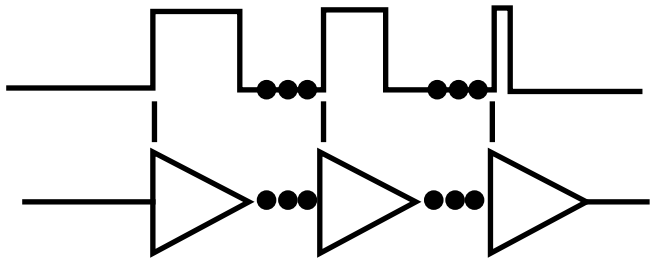
All gates have asymmetric response with regard to their rising and falling edges.

A pulse that propagates through a gate is either shortened (**pulse width compression**) or lengthened (**pulse width expansion**).

As a chain of gates gets longer, the level of **pulse width distortion** adds.

For example, assume the input pulse is *positive-going* and assume the delay of the rising edge exceeds the delay of the falling edge.

The succession of positive pulses will become increasing shorter, and eventually disappear for long strings of buffers.



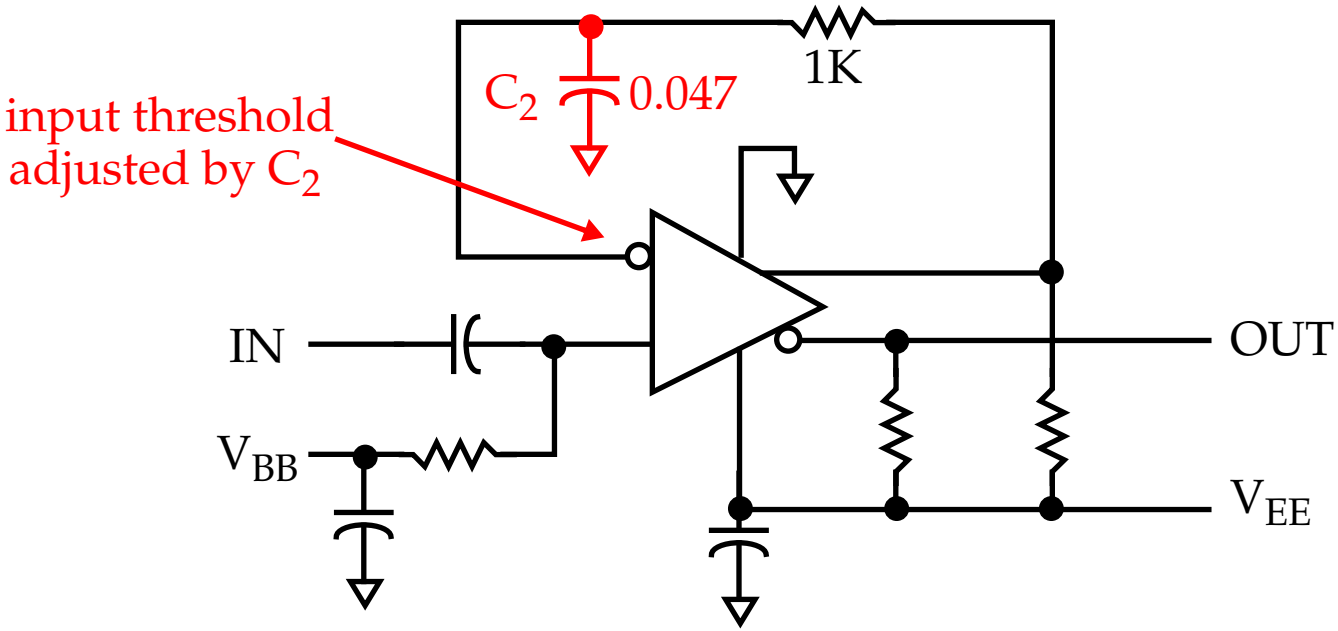
Clock Signal Duty Cycle

Two tricks can be used to solve this problem.

- Invert the clock signal at every stage in an **inverting chain**.

  This converts rising edges to falling ones and cancels pulse width compression in adjacent stages, over that of a non-inverting chain.

- Use an analog circuit that tracks the *average DC* value.



This only works with logic that has symmetric switching thresholds.

Clock Signal Duty Cycle

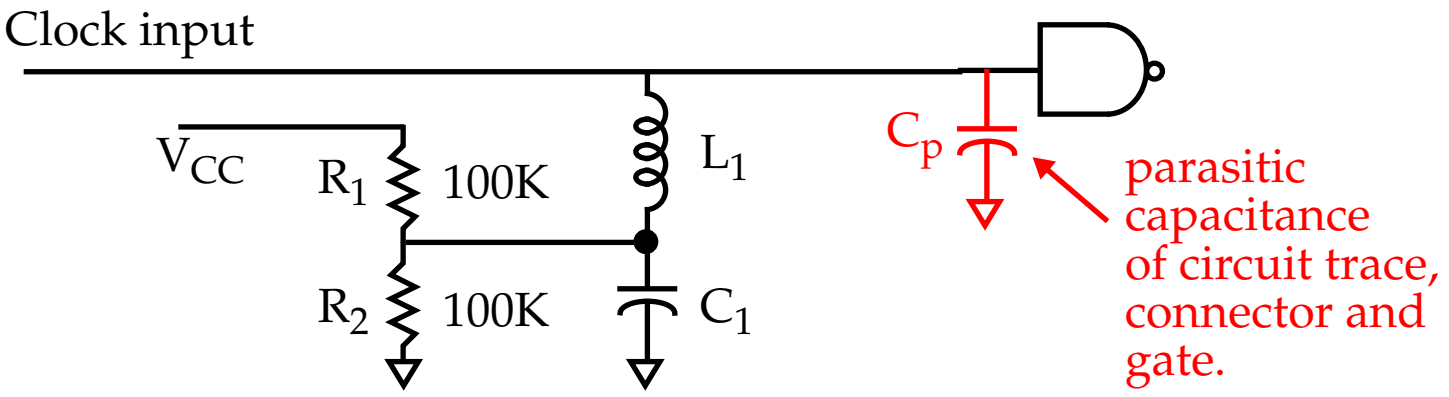
This circuit computes the average DC value and stores it on C_2.

The value on C_2 adjusts the *input switching threshold* to achieve an output duty cycle closer to 50%.

Canceling Parasitic Capacitance of Clock Repeaters

Adding a device to the clock wire adds parasitic capacitance, which shifts the received clock phase on all devices on the line.

This circuit can be used to combat the parasitic capacitance.



Canceling Parasitic Capacitance of Clock Repeaters

The *inductor* presents a **negative reactance** at the clock frequency and partially cancels the parasitic capacitance of the clk receiver circuit.

This is called a **matching network.**

Note the inductor-cancellation trick works only at the *fundamental frequency*, higher harmonics get no relief.

Be sure to use a clk driver with slow rise and fall times.

Such clks have lower harmonic content (more sinusoidal-like) and the neutralizing effect works better.

The two resistors are optional.

However, when used in a *hot plugging* environment, if they are absent, then a surge of current to charge C_1 will distort the clock signal.

A properly designed hot plug card receives power before touching the clock bus, and therefore, the resistors, if present, provide the charging current.

Canceling Parasitic Capacitance of Clock Repeaters

Keeping C_1 small helps shorten the precharge time.

The minimum value for C_1 is about 100 times C_p.

$$C_1 = 100C_p$$

$$L_1 = \frac{1}{(2\pi f)^2 C_1} + \frac{1}{(2\pi f)^2 C_p}$$

With R_1 and R_2 present, the precharge time to bring C_1 within 1% of its final value, (HI+LO)/2, is given as:

$$t_{pc} = 4.6\frac{R_1 R_2}{R_1 + R_2}C_1$$

Decoupling Clock Receivers from the Clock Bus

Clock taps on the clk bus can seriously distort the clk wfm.

Occurs when there are lots of taps, when the taps have large cap or when operating at high speed.

Decoupling Clock Receivers from the Clock Bus

One way to reduce the impact is to build a 3:1 attenuator at the input to each clock gate (receiver).

This will require more voltage gain in each clk receiver.

The attenuation network is inserted in series with clk receiver, at an impedance that is twice that of the receiver at the clock frequency.

This effectively triples the apparent input impedance of the receiver.

It also reduces the voltage to be interpreted by the receiver, but most gates have a lot of excess voltage gain.

Differential receiver circuits are commonly used here, which have plenty of gain and a precisely controlled input-switching threshold.