Digital Systems Design

Instructor:

Professor Jim Plusquellic

Text:

Howard Johnson and Martin Graham, "High-Speed Digital Design: A Handbook of Black Magic", Prentice Hall, 1993 (ISBN:0133957241)

Supplementary text:

Stephen H. Hall, Garrett W. Hall and James A. McCall, "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices", Wiley, 2000 (ISBN:0471360902)

Web: http://www.cs.umbc.edu/~plusquel/650

Course Description

This course covers:

- Fundamentals of systems design.
- High-speed properties of logic gates.
- Measurement techniques.
- Transmission lines.
- Ground planes and layer stacking.
- Terminations, vias and power systems.
- Connectors, ribbon cables, clock distribution and clk oscillators.

Prerequisites:

Basic Circuit Theory.
Experience with SPICE.
Familiarity with Test&Measurement equipment.
Some experimental background.

High Speed Digital Design

Focus is on the behavior of the passive circuit elements, i.e., wires, PCBs, packages.

And how these elements affect:

- Signal propagation (ringing and reflections)
- Interactions between signals (crosstalk)
- Interactions with external world (EMI).

The impedance (resistance) of a wire is frequency dependent, i.e., low resistance for low frequencies, high resistance for high frequencies.

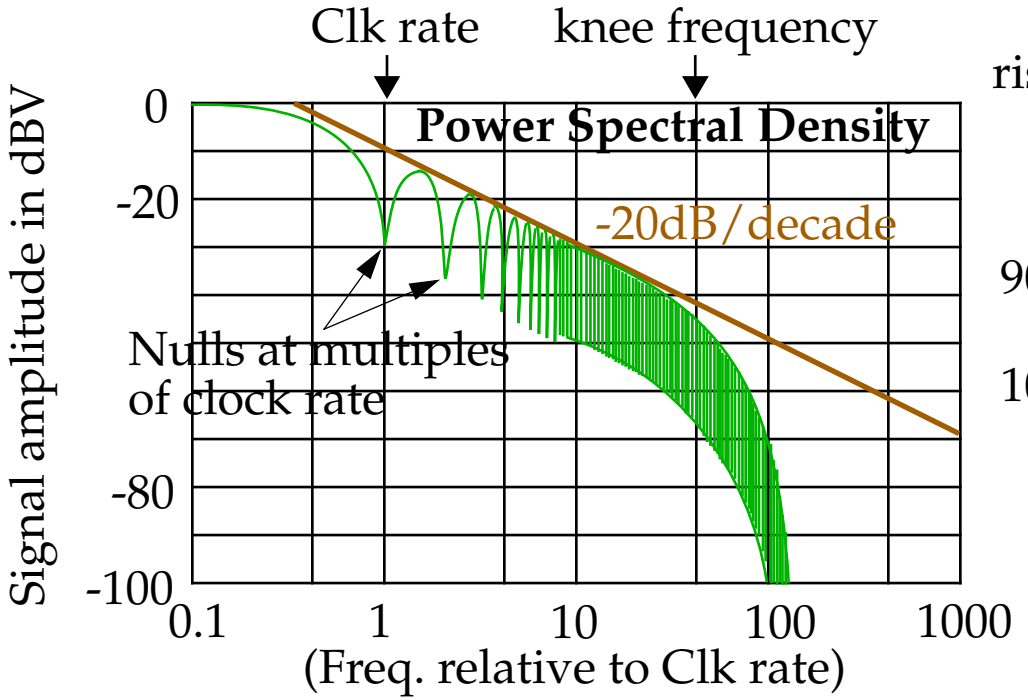
Electrical parameters are frequency dependent, most are not valid across more than 10 frequency decades.

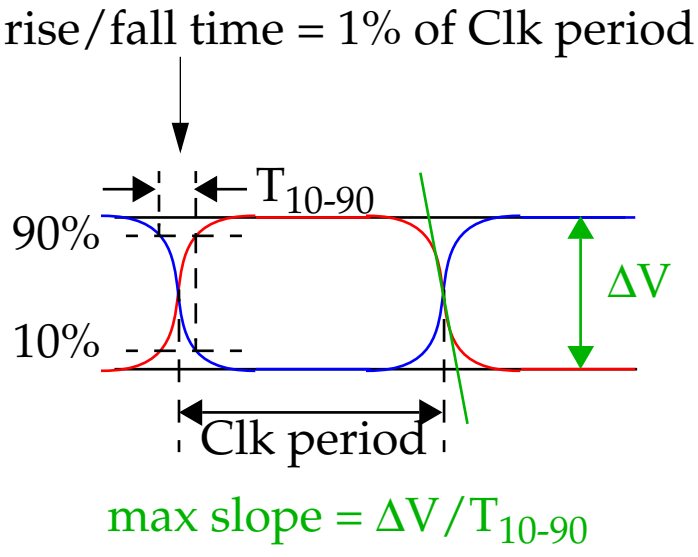
For example, a wire with 0.01 Ω at 1kHz increases to 1.0 Ω (skin effect) and 50 Ω of inductive reactance at 1 GHz.

For high speed digital design, what are the important frequency components?

Frequency and Time

The curve follows a -20dB/decade slope up to F_{knee}.





Most of the energy in digital pulses occurs below frequency:

$F_{knee} = 0.5/T_r$

F_{knee} is the highest frequency of concern in step input.

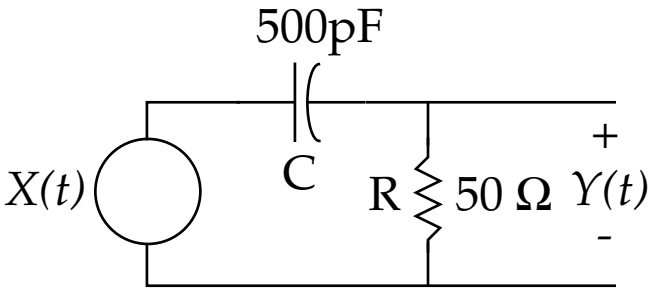
F_{knee} increases with smaller values for T_r.

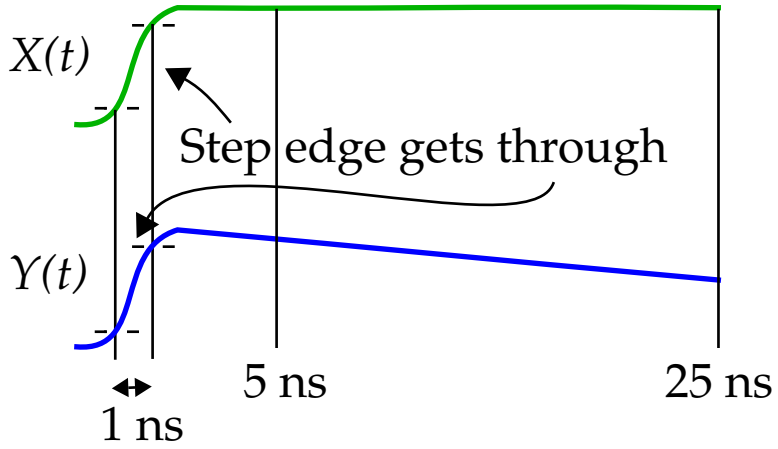
Frequency and Time

Any circuit that has a **flat** frequency response up to F_{knee} will pass a digital signal virtually unchanged.

If it's not flat, it will distort the signal.

For example, high pass filter:





At time t = 1ns (1GHz), reactance is 0.6 Ω, at t = 5ns (200MHz), reactance is 3 Ω and at t = 25ns (20MHz), reactance is 15 Ω.

$$X_C = \frac{1}{2\pi F_{knee} C} = \frac{T_r}{\pi C} = 0.6\Omega$$

Frequency and Distance

Electric signals propagate at speeds dependent on their surrounding medium.

Propagation delay: picoseconds/inch. Propagation speed: inches/picosecond.

Medium	Delay (ps/in)	Dielectric constant
Air (radio waves)	85	1.0
Coax cable (75% velocity)	113	1.8
Coax cable (66% velocity)	129	2.3
FR4 PCB: outer trace	140-180	2.8-4.5
FR4 PCB: inner trace	180	4.5
Alumina PCB: inner trace	240-270	8-10

Propagation delay increases in proportion to the **square root** of the dielectric constant of the surrounding medium.

Lower dielectric constants also reduce dielectric losses.

Frequency and Distance

Propagation delay of PCBs depends both on the dielectric material of the PCB and the trace geometry.

For example, the electric field of inner traces surrounded by ground planes stays in the board, which increases their propagation delay over outer traces.

Outer trace dielectric constant ~(1.0 + 4.5)/2.

Lumped versus Distributed Delay:

The response of a conductor to an incoming signal depends on whether the conductor is *smaller* than the effective length of the **fastest** electrical feature in the signal.

The effective length of an electrical feature, e.g. rising edge, depends on the time duration of the feature and its propagation delay.

Lumped versus Distributed Delay

For example, the rising edge of a ECL gate has a rise time of ~1ns.

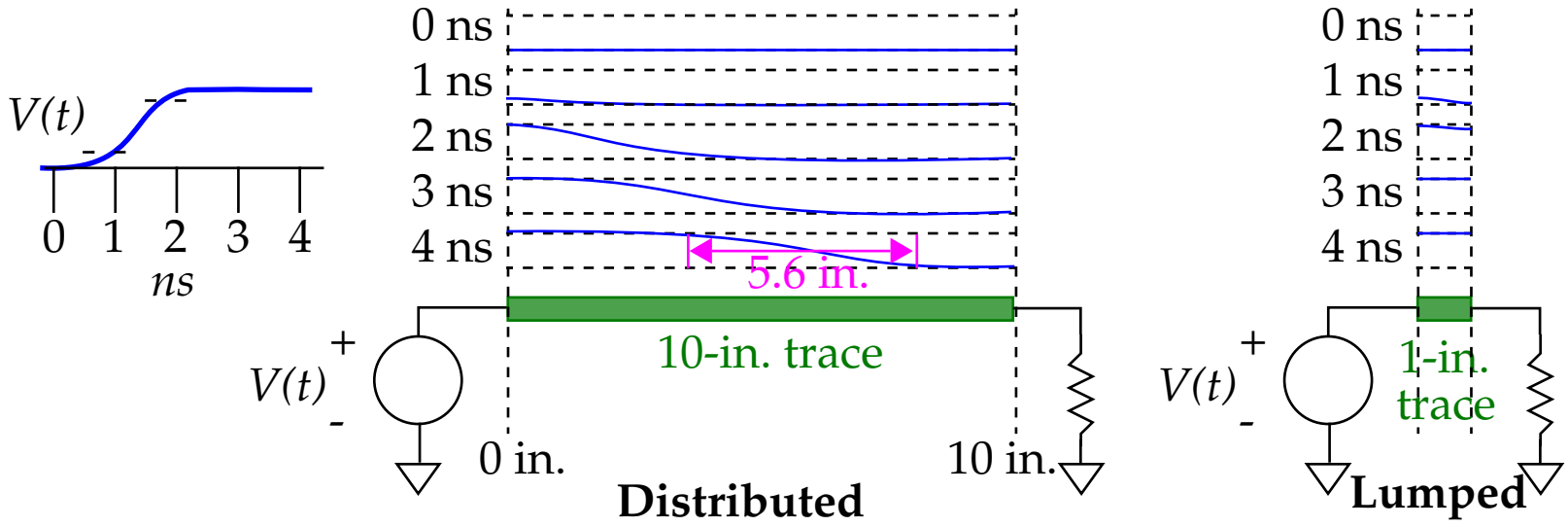
If propagating along an inner trace of a FR-4 PCB, it has an effective length of 5.6 in.

$$l = \frac{T_r}{D} = \frac{1000}{180} = 5.6 \text{ in.}$$

where l = length of rising edge in inches.

T_r = rise time in ps.

D = delay in ps/inch.



Lumped versus Distributed Delay

Distributed systems: The pulse propagates along the trace, the potential is ***not*** uniform at all points.

Lumped systems: All points react together with uniform potential.

Note that the classification of a system as lumped or distributed depends on the rise time of the signal.

The critical factor is the ratio of the wires length to the length of the rise-time.

For PCB traces, if the wire is shorter than 1/6 the effective length of the rising edge, the circuit is considered **lumped**.

Other thresholds commonly used:

- l/sqrt(2*pi)
- $l/4$