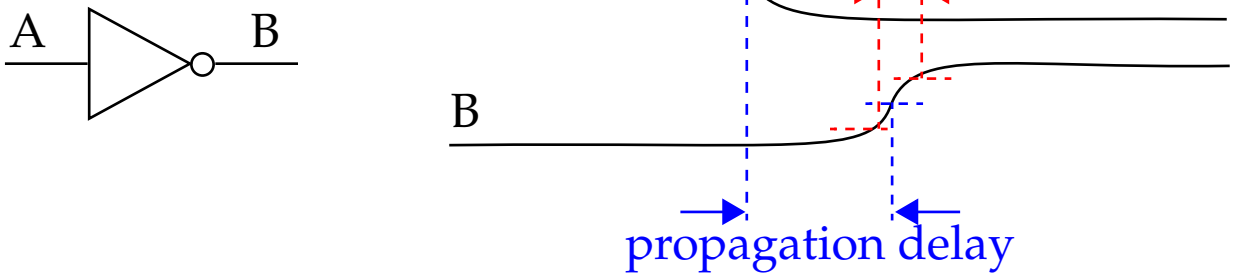
Speed

VLSI focuses on *propagation delay*, in contrast to digital systems design which focuses on *switching time*:



Faster switching times introduce problems independent of delay, e.g.,

- Return currents
- Crosstalk
- Ringing

Logic families that have switching times much faster than the propagation delay require attention to device packaging, board layout, connectors, etc.

Different logic families offer different *speed-power* combinations, e.g., TTL LS (low power Schottky), CMOS and ECL.

Speed

Manufacturers give speed and power on the data sheet because it's easy to characterize, but don't often list the **minimum switching time**.

More recently, manufacturers have introduced "edge-slowing" circuits, since fast edges cause problems through two distinct mechanisms.

Effects of sudden change in voltage, dV/dt:

Remember that most of the frequency content of a digital signal lies below the knee frequency, F_{knee}.

$$F_{knee} = \frac{0.5}{T_r}$$

This requires that device packaging, board layout and connectors have a "flat" frequency response up to at least F_{knee}.

Circuits that don't will distort the wfm at the receiver by reducing rise times, and adding lumps, overshoot and ringing.

Speed

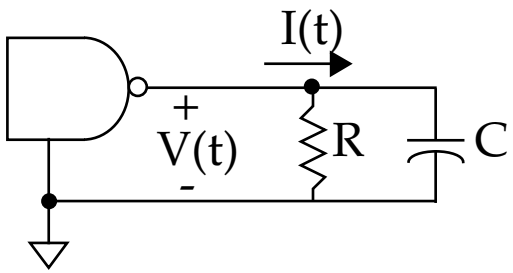
Effects of sudden change in voltage, dV/dt:

Of course, reducing rise time increases dV/dt, and F_{knee}.

dV/dt also increases crosstalk (via mutual capacitance).

Effects of sudden change in current, dI/dt:

We need to first estimate the rate of change in current in the source net.



Applying KCL:

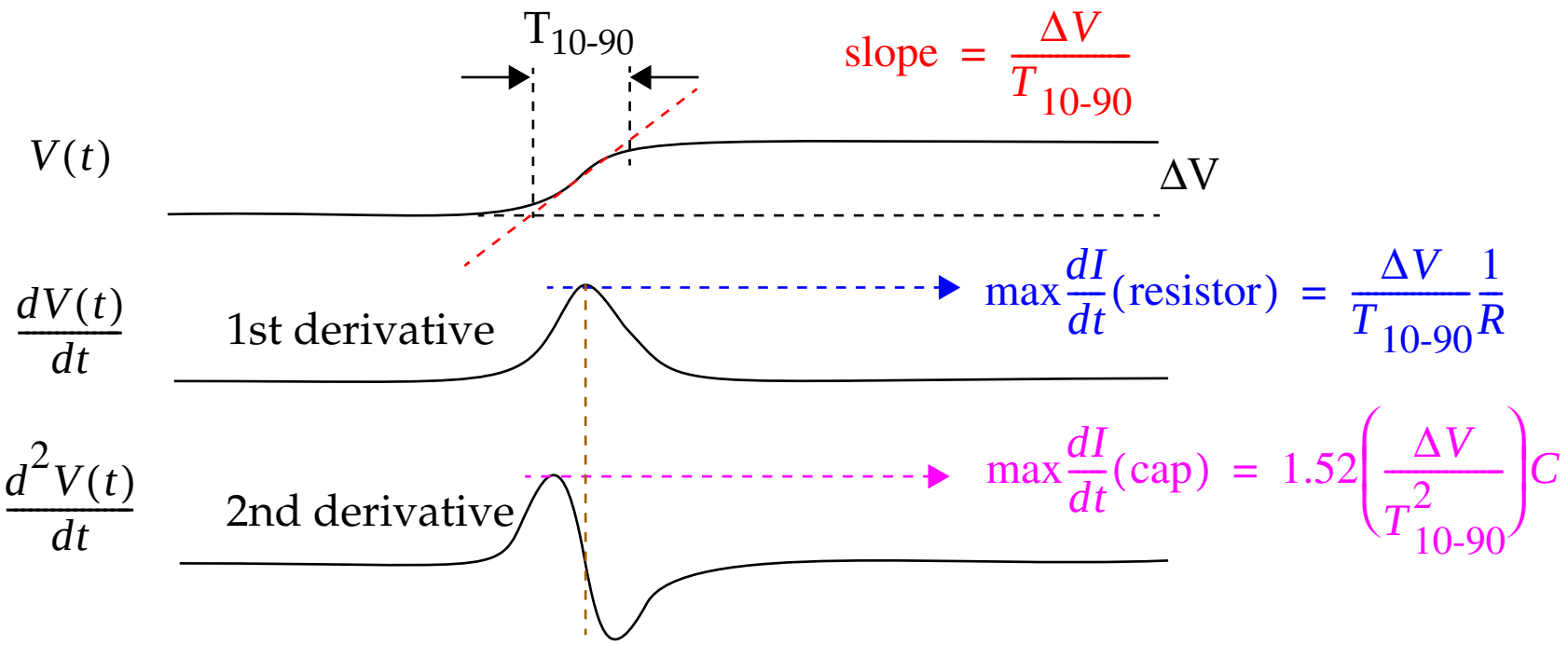
$$I(t) = \frac{V(t)}{R} + C\left(\frac{dV(t)}{dt}\right)$$

Differentiating gives the rate of change in current:

$$\frac{dI(t)}{dt} = \frac{1}{R}\left(\frac{dV(t)}{dt}\right) + C\left(\frac{d^2V(t)}{dt^2}\right)$$

Speed

We need to do this since the oscilloscope reads out voltage, not current.



These equations yield the **maximum** rate of change in current in the resistor (1st derivative) and capacitor (2nd derivative).

An estimate of the maximum is given by the *sum* of these components, which overestimates a bit since the peaks don't line up (phase differences).

Speed

Note that this analysis indicates why mutual inductance is such a problem.

Here, the rate of change in current is proportional to 1 over the square of the 10-90% rise time.

Therefore, cutting the rise time in half **quadruples** the amount of dI/dt flowing into capacitive loads.

Rate of change in a TTL output current:

Assume load is capacitive: C_L = 50 pF, ΔV is 3.7 V and T_r = 2 ns.

$$\frac{dI}{dt} = \frac{1.52 C_L \Delta V}{T_r^2} = 7.0 \times 10^7 A/s$$

Rate of change in a ECL output current (faster and generates less noise!):

Assume load is resistive: R_L = 50 Ω, ΔV = 1.0 V and T_r = 0.7 ns.

$$\frac{dI}{dt} = \frac{\Delta V}{R_L T_r} = 2.8 \times 10^7 A/s$$

Speed

Voltage margins: difference between guaranteed output of a logic driver and the worst-case sensitivity of a logic receiver.

This is analogous with our treatment of noise margins in VLSI.

For example, V_{IL} min indicates, across **all** gates, the *minimum* value of V_{IL} that guarantees the receiving gate will interpret the signal as low.

Noise margins are V_{OH} - V_{IH} or V_{IL} - V_{OL}, whichever is smaller.

Margins guarantee proper operation in the presence of signal corruption:

- DC power supply currents change ground reference voltages between sending and receiving gates.
- Fast changing return signal currents flowing through the inductance of a ground path, also cause ground voltage differentials.
- Coupling via mutual capacitance and inductance.
- Ringing (reflection) on long lines distort edge at receiver.
- Temperature variations between chips change thresholds.

Speed

Items 1-5 apply to all systems while items 2-4 are relevant to high-speed systems.

The degree of signal corruption is proportional to the magnitude of the transmitted signal in each of these.

A measure of tolerance to effects 2-4 for a logic family is expressed as the ratio of noise margins to the voltage output swing:

$$\frac{V_{OH}\ \text{min} - V_{IH}}{V_{OH}\ \text{max} - V_{OL}\ \text{min}} \longleftarrow \text{margin} \longrightarrow \frac{V_{IL} - V_{OL}\ \text{max}}{V_{OH}\ \text{max} - V_{OL}\ \text{min}}$$

$$\longleftarrow \text{V swing} \longrightarrow$$

For example, even though the actual margins in ECL are smaller, the percentage is 13.2% vs 9.1% for TTL.

Therefore, ECL logic has better noise immunity than TTL.

However, ECL (10KH) switches 2-3 times faster than the 74AS family.

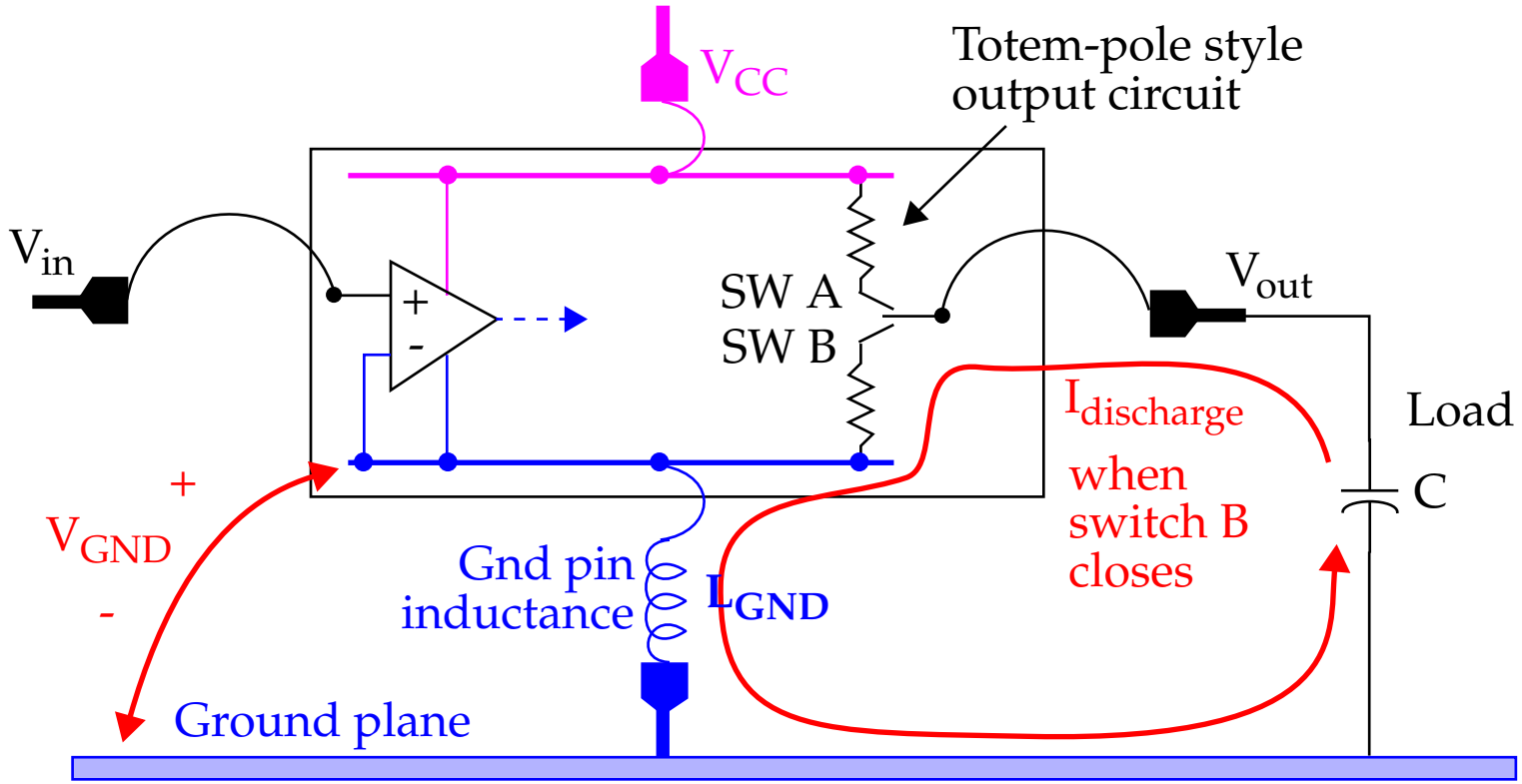
This increases the return-current, crosstalk and ringing.

Packages

All packages suffer from problems with *lead inductance*, *lead capacitance* and *heat dissipation* at high speeds.

Lead inductance causes ground bounce.

This causes glitches in the logic inputs whenever the device outputs switch.



Ground Bounce

The stored charge on load capacitance, C, flows into ground when switch B closes.

The increase in current followed by a decrease in current induce a voltage, V_{GND} between the system ground plane and the device GND.

This shift in ground voltage in the device due to the output switching is called *ground bounce*:

$$V_{GND} = L_{GND}\frac{dI_{\text{discharge}}}{dt}$$

The magnitude of the ground bounce, V_{GND}, is usually small compared with the output voltage swing and does not impair transmission.

However, it interferes with signal reception at the inputs significantly.

Ground Bounce

For example, the input receiver *differentially* compares the input voltage, V_{in}, with its local ground reference.

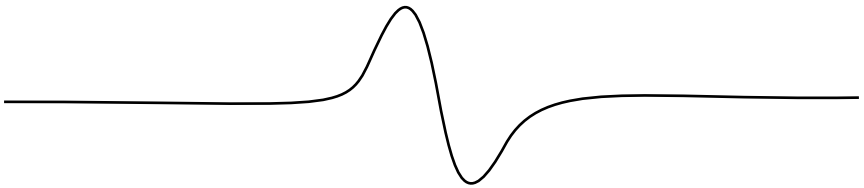
With a V_{GND} noise pulse appearing, the input circuit sees V_{in} - V_{GND} and responds to it.

It cannot distinguish, for example, between a fall in V_{in} or a raise in V_{GND}, i.e., the effect is equivalent to introducing noise on the input.

V_{GND} is amplified by N when N outputs switch simultaneously.

Ground bounce voltages are proportional to the *rate of change in current* through the ground pin.

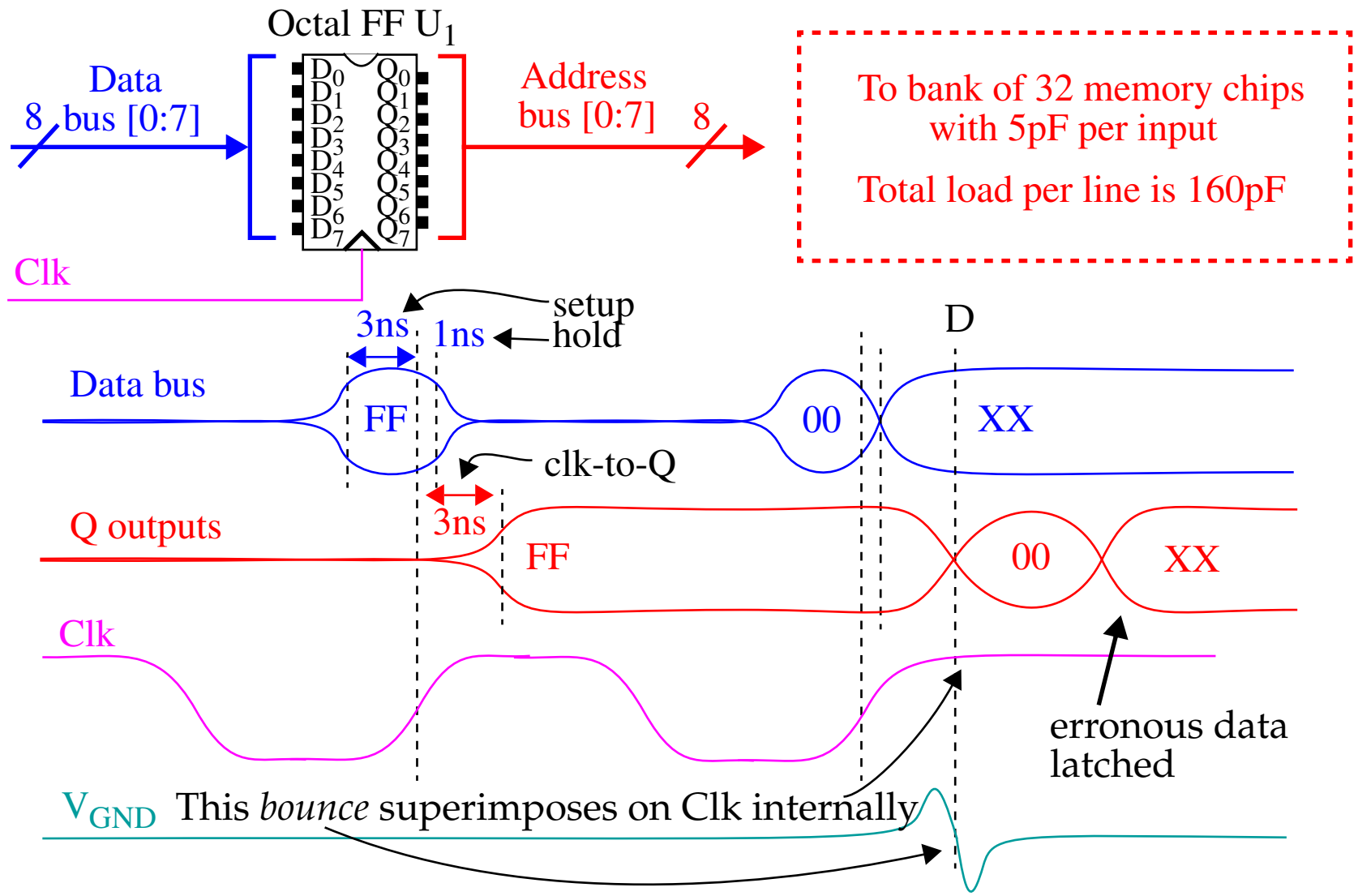
Capacitive loads cause the rate of change in current to look like the 2nd derivative of the voltage.



$$|V_{GND}| = \frac{1.52\Delta V}{(T_{10\text{-}90})^2} C$$

Ground Bounce

The ground bounce at time *D* causes don't care data XX to overwrite 00.



Ground Bounce

The noise pulse causes an error called *double clocking*.

The FFs reclock themselves in the presence of the pulse.

Note: external observations of Clk would show a perfectly clean signal -- the pulse manifests ONLY internal to the package (see text for an example).

Surface mounted packages, with shorter pins and less inductance, are less susceptible.

Some manufacturers provide special **power pins** for the output drivers.

This fixes the problem.

In order to predict ground bounce, 4 pieces of information are needed.

- The 10-90% switching time of the driver
- The load capacitance or load resistance
- The lead inductance
- The magnitude of the switching voltage

Ground Bounce

For resistive loads, first compute the rate of change in current (as we did before) and then apply the definition of inductance:

$$|V_{GND}| = L\frac{\Delta V}{T_{10\text{-}90}}\frac{1}{R}$$

For capacitance loads:

$$|V_{GND}| = L\frac{\Delta V}{T_{10\text{-}90}^{2}}C$$

Text gives ΔV and $T_{10\text{-}90}$ for various logic families.

Ground lead inductance is a strong function of package type.

Internal package ground planes help.

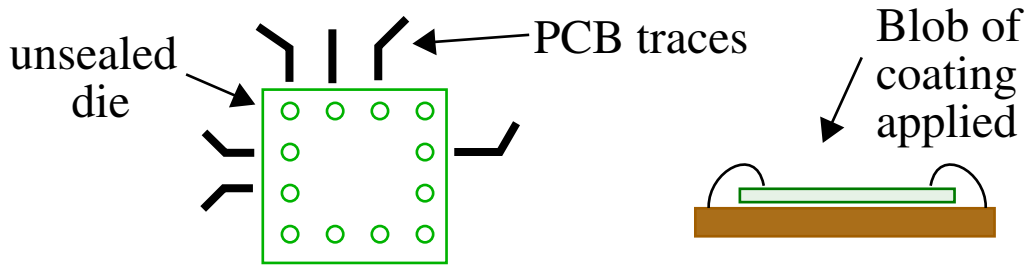
Better techniques include:

- Wire bond
- Tape automated bonding (TAB)
- Flip-chip

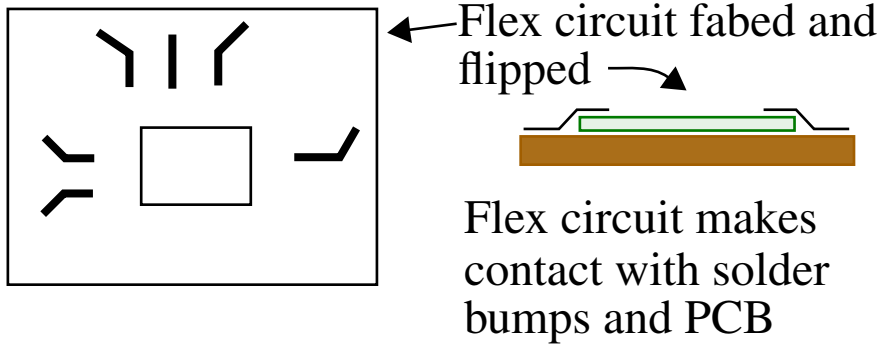
Package Types

Flex circuit different for each chip in TAB technique.

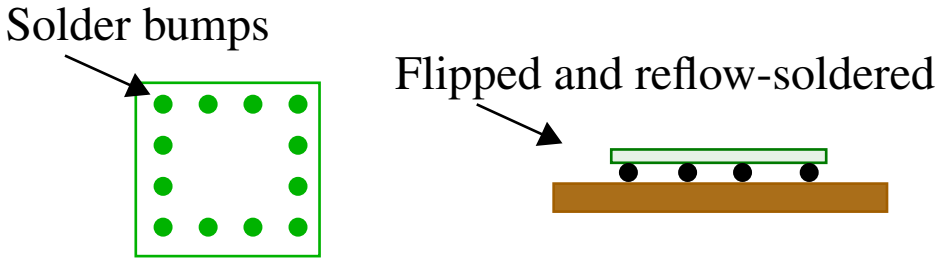
Wire bond



Tape Automated Bonding



Flip-chip
(package parasitics are minimal)



Flip-chip has no mechanical compliance between chip and PCB requiring closely matched thermal coefficients of expansion.

Ground Bounce

For comparison, lead inductance is:

- ~8 nH for 14-pin plastic DIPs
- ~1 nH for wire bond
- ~0.1 nH for fl ip-chip bond

Slowing down the edge transition time reduces ground bounce.

For example, 10K ECL family incorporate circuitry to do this with minimal impact on propagation delay.

Multiple, evenly spaced, grounds around the chip helps too.

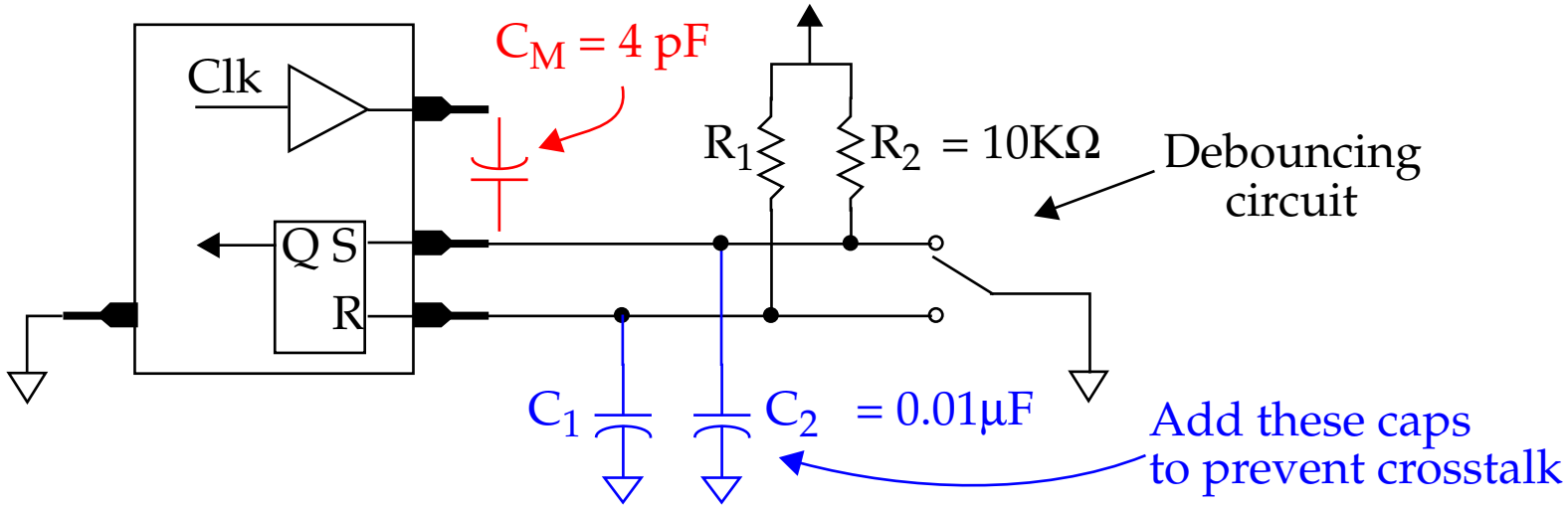
The 10K ECL family provide a *ground sense pin* and an internal reference voltage generator, which has a direct path to an external ground.

This pin does not carry large ground currents and therefore, acquires no ground bounce.

Differential inputs are similar to this technique, but are even more effective.

Lead Capacitance

Stray capacitance between pins of a logic device can couple noise voltage onto inputs.



We derived the percentage crosstalk previously with C_M known:

$$I_M = C_M \frac{\Delta V}{T_r} \longrightarrow \text{Crosstalk} = \frac{R_B I_M}{\Delta V} = \frac{R_B C_M}{T_r} = \frac{10k \times 4p}{5n} = 8!$$

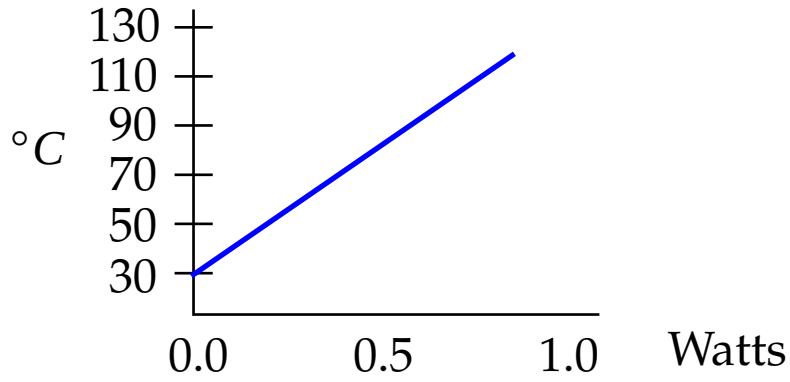
(assumes no capacitance on victim)

Crosstalk with caps C_x is just equal to ratio of mutual to grounded cap:

$$\text{Crosstalk} = C_M / C_1 = 4p/10n = 0.0004$$

Heat Transfer

The relationship between temperature and power is typically linear for all types of packages.



Therefore, the *junction temperature* (temperature inside the device) is porportional to the power dissipation *P*.

$$T_{\text{junction}} = T_{\text{ambient}} + \Theta_{JA} P$$

The offset is the ambient temperature and Θ_{JA} is equal to the *thermal resistance*.

Θ_{JA} is a function of the die attachment method, the package material and size and any special heat dissipation features such as fins or wings.

Heat Transfer

The thermal resistance, Θ, is often partitioned by the manufacturer into:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$$

with $\Theta_{JC} = \Theta$ from *junction* to the package *case* and
with $\Theta_{CA} = \Theta$ from the package *case* to *ambient* environment.

Usually, you can do nothing about Θ_{JC} but you can treat Θ_{CA}.

Heat sink manufacturer's give the specs for Θ_{CA} of their heat sinks.

Heat sinks dissipate heat by adding surface area and forced air fl ow

Making a heat sink 40% larger in all dimensions halves the Θ_{CA}.

Air fl owsof 400 ft/min are approximately equal to 4.5 miles/hr, which is a challenging spec to achieve in a computer chasis.

Text elaborates on this topic.