Trojans II(A)

1) Name the three technical domains that need to be considered by path delay-based HT detection methods

Multiple choice:

1) A golden-model analysis refers to

a) A method where chip data is compared with itself
b) A method where chip data is compared with data generated by simulations
c) A method where simulation data is compared with simulation data from other process corners
d) A method where simulation data is compared with itself

2) The observer effect with respect to HTs refers to

a) The act of observing a system using a HT trigger for example changes it behavior
b) An act carried out but an adversary once the HT is activated
c) The act of having one chip monitor the behavior of another
d) The interference introduced by a system when the chip is opertional in the field

Trojans II(B)
1) The main drawback of LOS and LOC used for delay testing is

Multiple choice:
1) Path delay testing is characterized by all of the following except
a) Two vectors that are applied consecutatively to the PIs of the functional unit
b) A timed test that is carried out after the vector V2 of the 2 vector sequence is applied to the PIs of the functional unit
c) A launch event that inverts the input bits to the functional unit
d) A capture event that samples the functional unit outputs after a specific delta-t

2) Scan is characterized by all of the following except
a) A second serial path through the FFs of the chip
b) The addition of SI, SE and SO pins to the chip to enable external access to the scan chain
c) The addition of a 2-to-1 MUX inserted in the functional path with output connect to the FF inputs
d) A sequence of FFs that are connected such that their outputs are connected to their inputs through a MUX

Trojans II(C)
1) How is the vector V2 in a 2 vector sequence for Launch-on-Shift (LOS) derived?

Multiple choice:
1) Manufacturing delay tests do not measure the actual individual path delays but rather
a) Apply tests that are designed to decide the lower bound on the delays of all paths in the chip
b) Apply tests that are designed to decide the upper bound on the delays of all paths in the chip
c) Apply tests that measure the shortest path through each node
d) Apply tests that test for nodes that have an infinite delay associated with them

2) The individual edges associated with a glitch in a combinational circuit correspond to
a) The delays from the same path where the path being tested is unstable
b) The delays through a set of FFs
c) The delays of feedback paths
d) The delays of various subpaths in the circuit

Trojans II(D)
1) Undesirable power supply noise occurs in clock sweeping methods because

Multiple choice:
1) The following is true regarding false positives for detects and HTs except
a) False positives are easier to avoid in defect testing than they are in HT detection methods
b) False positives are more common in HT detection methods because precise delay measurements are made in HT detection methods
c) False positives can be more expensive for defect testing than they are for HT detection methods
d) False positives can occur in HT detection methods if the statistical detection method does not account for process variations properly

2) A single clock timing scheme is also called
a) Clock sweeping
b) Clock strobing
c) Clock injection
d) Clock inversion

Trojans II(E)
1) Describe a drawback of the RO timing scheme

2) Name a significant benefit of REBEL over other timing scheme

Multiple choice:
1) The dual clock timing scheme reduces power supply noise because
a) It never generates any clock edges
b) It couples the two clocks, cancelling the noise that would be generated
c) Only three clock edges are ever closely spaced in time
d) Only two clock edges are ever closely spaced in time

2) The TDC timing scheme detects hazards by
a) Inspecting the thermometer code for an invalid value
b) Using a filter that prevents them from entering the TDC
c) Using an XOR gate that produces a 1 when two or more edges occur
d) Using EdgeCnters which counts the number of edges that occur on each input

Trojans II(F)

Multiple choice:

1) The following is true regarding the REBEL embedded test structure except
a) The existing FFs in the design are used to create a delay chain
b) FFs preceeding the insertion point are used to encode the insertion point
c) The slave latches in the FFs are used to create the delay chain
d) The delay chain captures a digital snapshot of a signal's temporal behavior

2) The following approaches can be used as the statistical detection method for HTs except
a) GoldenSim-based
b) PCM-based
c) Chip-Centric
d) Model-building

Trojans II(G)

Multiple choice:

1) The transition fault model (TDF) and path delay fault (PDF) model are different because
a) The TDF model assumes defects are lumped on each node while the PDF model assumes defects are distributed along the entire path
b) The TDF model times only the transition at the node of interest while the PDF model times an entire path
c) The TDF model is based on hazard-free circuit structures while the PDF model is based on any type of circuit structure
d) The TDF model is based the behavior of older technologies while the PDF model is modern

2) The TDF model when used for HT detection targets the shortest path through each node because
a) It is faster to apply the tests
b) Power supply noise is reduced because fewer logic gates are involved in the signal propagation
c) It is easier to determine the 2 vector sequence that times shorter paths than it is for longer paths
d) The delay anomaly created by a HT is largest as a fraction of the overall path delay and therefore is more easily detected