Characterizing Within-Die Variation from Multiple Supply Port IDDQ Measurements

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Abstract — The importance of within-die process variation and its impact on product yield has increased significantly with scaling. Within-die variation is typically monitored by embedding characterization circuits in product chips. In this work, we propose a minimally-invasive, low-overhead technique for characterizing within-die variation. The proposed technique monitors within-die variation by measuring quiescent (I_{DDQ}) currents at multiple power supply ports during wafer-probe test. We show that the spatially distributed nature of power ports enables spatial observation of process variation. We demonstrate our methodology on an experimental test-chip fabricated in 65-nm technology. The measurement results show that the I_{DDQ} currents drawn by multiple power supply ports correlate very well with the variation trends introduced by state-dependent leakage patterns.

Keywords: Process Variation, IDDQ, Characterization, DFM

I. INTRODUCTION

Process variation is typically observed at several different scales such as lot-to-lot, wafer-to-wafer, across wafer and across-field variation. Lot-to-lot and wafer-to-wafer variations are caused by long-term drifts in tools and wafer processing conditions. Across-wafer variation primarily occurs due to wafer-level non-uniformities such as post exposure bake (PEB) temperature gradient [1] and resist thickness variation [2]. Across-field variation, on the other hand, stems from optical sources such as across-field focus and dose variation [3] and mask errors [4]. In addition to the above sources, across-die variation can also be caused by layout dependent systematic effects such as pitch and density dependent line-width variability [5,6] and microscopic etch loading [7].

Different components of variation are routinely monitored in a manufacturing line to predict the health of the line. Large scale variations such as lot-to-lot, wafer-to-wafer, and to a certain extent, across-wafer variation can be adequately monitored by measurements taken from scribe line (physical space between dies allocated for dicing purposes) test structures [8]. These scribe line structures contain a range of test macros required for monitoring different sources and components of variation. However, the scribe-line macros do not provide any coverage of within-die variation. In order to monitor within-die variation, one must place supplemental test circuits on product dies. These structures should be spatially distributed across the 2-dimensional plane of the die to obtain sufficient spatial coverage. This places significant restrictions on the kind, number, and location of the test structures that can be embedded in a chip. This is true because any structure embedded in a product chip should be minimally invasive while adhering to strict design and test limitations such as acceptable power, area, I/O interface, and test-cost.

There has been a significant body of work in the area of test structure design and process monitoring [9,10,11]. However, due to limitations discussed above, on-product monitors have barely evolved beyond embedded ring oscillators. These ring oscillators are usually placed at multiple locations and their frequencies can be routinely measured to reflect within-die variation. The ring oscillators are usually identical in nature or they can be tuned to cover different circuit styles or heighten their sensitivity to a particular process parameter [12,13].

Figure 1 shows the layout of a chip with twelve embedded ring oscillators [14]. The ring oscillators are identical in design and are distributed across the area of the chip in a fairly regular manner. Figure 2 shows the measured data where each ring frequency is plotted with respect to the ring located in the upper-right corner [14]. The lack of correlation in the measured frequencies of the spatially separated ring oscillators clearly reflects the significance of across-die variation.

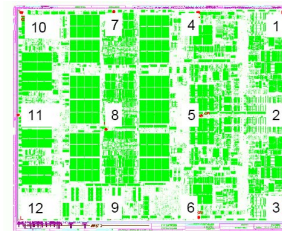**Figure 1: Layout of a chip with markers indicating the physical locations of twelve embedded ring oscillators [14].**
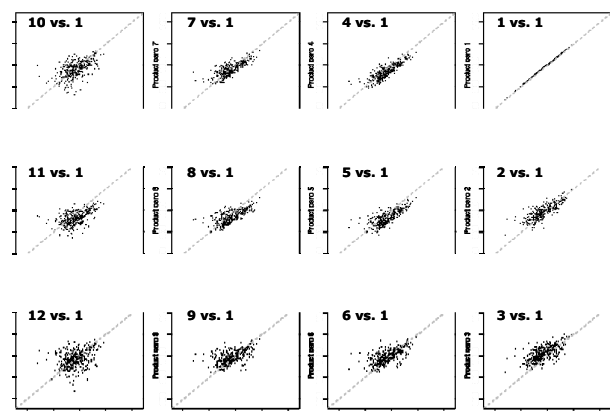

Figure 2: Scatter plot of the twelve ring oscillator frequencies with respect to the ring in the upper most corner [14].

In this paper, we present a minimally-invasive approach for monitoring within-die variation. Our approach is based on quiescent current (I_{DDQ}) measurements. In the proposed method, individual I_{DDQ} measurements are made at multiple supply ports that are spatially distributed across the area of the chip. The within-die variation profile is extracted from the multiple supply port I_{DDQ} signature. We show that the multiple supply port I_{DDQ} signature, which is a measure of how overall chip I_{DDQ} is distributed across different pads, correlates well with the within-die variation profile. We present experimental hardware data from a test-chip fabricated in 65-nm SOI technology to validate this correlation. We discuss the benefits of the proposed method and argue that it enables a low overhead and minimum perturbation characterization of within-die variability in product chips.

The proposed quiescent current-based method provides several benefits over embedded test structures:

- The method requires only a small on-die test structure to calibrate for resistance variations in the power grid (to be discussed) and therefore, it is minimally invasive. The area and design time overheads of the technique are very small.

- Multiple port I_{DDQ} measurements are made through power supply ports. Therefore, the method leverages the existing architectural component of the chip for data collection whereas embedded structures may require additional ports for measurements.

- Given that the spatial separation between supply ports is typically less than 500 microns in C4-based chips, and many ICs posses hundreds of such power ports, the technique provides a high level of resolution of with-in die leakage variation. The widely distributed nature of the power ports enables a chip-wide or a specific region-based analysis to be carried out.

- The technique requires no more tester time than other embedded test structures, such as the embedded ring oscillator scheme described previously, thereby enabling regular monitoring of within-die variation with minimal test-overhead.

- I_{DDQ} measurements are very robust in characterizing long-range spatial variations. This is true because I_{DDQ} measures the aggregate effect and thus naturally eliminates local random and local layout dependent effects.

The remainder of the paper is organized as follows. In the next section, we discuss the multiple supply port measurement technique and its application in characterizing within-die variation. Section III discusses extraction of across-die variation parameters from multiple supply port I_{DDQ} measurements. Finally we present hardware measurement results in Section IV and practical implementation issues in Section V before concluding in Section VI.

II. MUTIPLE SUPPLY PORT I_{DDQ} METHOD FOR SENSING ACROSS-DIE VARIATION

I_{DDQ} testing is a well known method for defect detection but the efficacy of I_{DDQ} testing has been diminished due to large background static leakage currents in current technologies. The problem is further exacerbated due to exponential dependence of leakage on process parameters such as channel length and threshold voltage. Process variation can cause an order of magnitude variation in chip leakage [15], thereby making it hard to isolate defect current from the leakage variation. However, in the absence of defects, chip-to-chip I_{DDQ} variation is a reliable indicator of die-to-die variation and can be used to extract chip-mean values of process parameters. The chip-wide I_{DDQ} does not contain information to extract within-die variation. A multiple supply port (MSP) measurement technique has previously

been proposed for defect testing [16]. In this section, we discuss the MSP measurement technique and show that it can be used to extract across die variation profile from I_{DDQ} measurements[1].

The power grids of most commercial products interface to an external power supply through multiple power ports. The interface can be through peripheral pads or through a C4 bump array, as shown in Figure 3. The power ports of the latter are distributed across the 2-dimensional plane of the chip to minimize IR and Ldi/dt voltage variations introduced by the finite resistance of the metal that defines the power grid[2]. The distributed nature of the power ports enables regional observation of the current distribution characteristics of the chip. The multiple supply port I_{DDQ} technique measures currents drawn from the individual power ports distributed across the surface of chip. The I_{DDQ} currents drawn from multiple ports reflect the regional composition of the overall chip-wide I_{DDQ}.
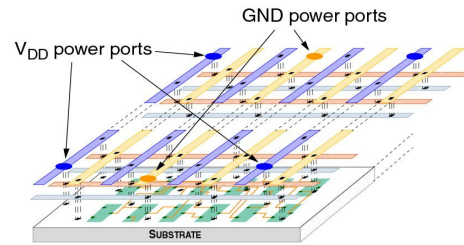

Figure 3: Multi-layer power grid with C4 bumps as power ports. The power ports are distributed across the 2-D plane of the chip.

Within-die variation is highly spatially correlated [17] and hence it impacts the regional distribution of I_{DDQ} by increasing leakage in the faster regions of a chip while reducing it in the slower regions. Within-die variation, therefore, modulates the I_{DDQ} currents drawn from spatially distributed power supply ports. For a chip with N power ports, we define a MSP I_{DDQ} ratio signature as an N-dimensional vector $\mathbf{Q}$:

$$\mathbf{Q} = \frac{1}{I_{DDQ}}\begin{bmatrix} I_1 & I_2 & .... & I_N \end{bmatrix}^T \tag{1}$$

Here I_{DDQ} represents total chip-wide leakage and I_1 to I_N represent the currents drawn from the N individual power supply ports. I_{DDQ} is the sum of individual leakage currents I_1 to I_N. The above signature essentially measures the relative contribution of each port to total chip leakage.

The intuition behind using the MSP I_{DDQ} signature to sense within-die variation is that if a specific region of a chip becomes slow or less leaky, then the MSP I_{DDQ} signature reflects this profile by having a lower relative leakage contribution in the ports supplying current to that region. Similarly, a faster or leaky region alters the MSP I_{DDQ} signature by increasing the leakage contribution of the neighboring ports. Figure 4 illustrates this concept with a hypothetical example of a chip with 8 supply ports located at the boundary of the chip. Figure 4 shows two scenarios: 1) there is no significant within-die variation and 2) there is a within-die variation trend with the left region of the chip being relatively faster (lower L_{eff} or lower V_T) than the right region. For the two scenarios shown in

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[1] I_{DDQ} is state-dependent. The appropriate state in which to place the chip for the most effective characterization of leakage can be determined in advance from simulations.

[2] Although a spatial with-in die characterization of leakage is possible for peripheral pad ICs, the resolution of the proposed technique is reduced over that available in C4-based chips because of the pad placement constraints.

Figure 4, it is possible that the overall chip I_{DDQ} for the two chips are comparable. The two I_{DDQ} currents will be comparable if in scenario 2, the increased leakage from the fast region of the chip compensates the reduced leakage from the slow region. However, if we compare the MSP I_{DDQ} ratio signatures for these two chips, the signatures will be distinctly different. For the within-die variation trend shown in scenario 2, the relative leakage contributions of the pads labeled L1, L2, T1 and B1 will increase at the expense of the reductions in the fraction of overall leakage that is contributed by the ports identified by labels R1, R2, T2 and B2 in the figure.
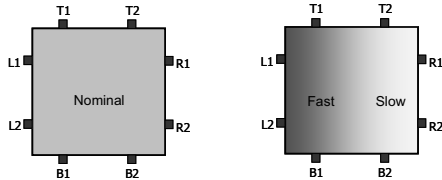

Figure 4: Illustrative example of a chip with 8 supply ports. The chip on the left has no within-die variation while the die on the right exhibits a within-die trend.
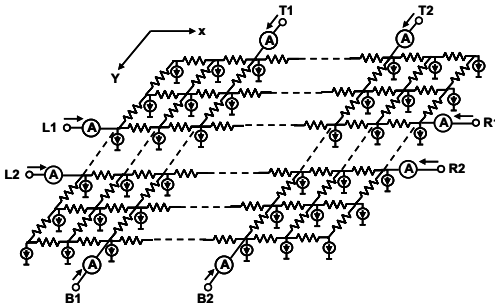

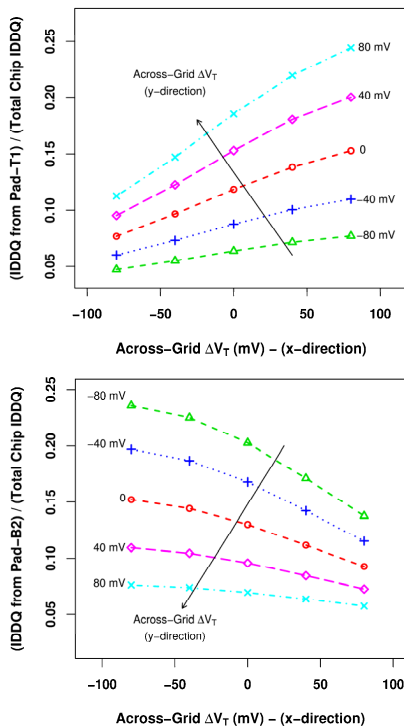**Figure 5: Experimental power grid with 8 supply ports. Individual currents through each supply port are measured.**

Figure 6: I_{DDQ} ratios for ports T1 (top) and B2 (bottom). Both x and y direction V_T trends modulate the I_{DDQ} ratios of the ports.

In order to verify the above observations, we setup a representative power grid with eight power supply ports located around the periphery of the chip. In practice, the device loads and hence the current demands across a real power grid are not symmetric. This is true because different regions of a chip may contain different circuit densities with varying leakage requirements. Moreover, the leakage of the logic gates is state dependent and will introduce variations. The experimental setup takes this into account by distributing asymmetric current loads across the grid. Figure 5 shows the experimental setup of the power grid with distributed resistances for DC analysis. We can simulate the grid under different conditions and obtain the currents drawn through each of the eight power ports shown in the figure.

First, we simulate this power grid and compute the MSP I_{DDQ} ratio signature with no within-die variation. Next, we artificially introduce linear threshold voltage (V_T) trends in both x and y-directions and compute the MSP I_{DDQ} ratio signatures for different values of within-die variations. Figure 6 shows the I_{DDQ} ratios for port T1 and port B2 respectively. In the figure, a negative value of x-direction ΔV_T indicates that the right side of the die has lower V_T (higher leakage) than that on the left side of the die. Similarly, a negative value of y-direction across-grid ΔV_T represents a V_T trend where devices in the lower part of the chip see lower V_T as compared to those in the top section. A zero value of ΔV_T for each direction indicates no across-die variation in the corresponding direction. The figure shows a clear impact of across-grid ΔV_T trends on the current ratios of port T1 and port B2. For example, as the y-direction ΔV_T goes from negative to positive, the current ratio for port T1 increases while the ratio for port B2 decreases. This is true because the leakage in the region surrounding port T1 increases while the leakage in the region neighboring port B2 decreases under these conditions. Similarly, in the x-direction, an increase in across-grid ΔV_T results in an increase in the current ratio for port T1 at the expense of a reduction in the I_{DDQ} ratio of port B2. Similar trends, though not shown in Figure 5, are also observed for other six ports. These trends indicate that the I_{DDQ} ratios for individual ports get modulated by the current demands in the vicinity of the ports.

Figure 7 shows the multiple port I_{DDQ} signatures for all eight ports for different across-grid variation profiles. The figure shows that different variation profiles produce distinctly different signatures thereby indicating that the I_{DDQ} ratio signature can be used to estimate within-die variability. We point out here that the sensitivity of MSP I_{DDQ} signature to with-in die variation depends on the ratios of power grid impedances between different power ports and spatial regions in a chip. The MSP technique does not rely on the absolute values of grid impedances and hence maintains its effectiveness for low impedance power grids. In the next section, we discuss how we can use the I_{DDQ} signature to extract within-die variation.

III. EXTRACTING ACROSS-DIE VARIATION FROM MUTIPLE SUPPLY PORT I_{DDQ} SIGNATURE

The multiple supply port I_{DDQ} signature can be mapped to a specific within-die variation profile. This mapping can be performed by building regression models of within-die variation parameters as a function of the I_{DDQ} signature. Let us consider a process parameter X (for example, L_{eff} or V_T). Let us assume that the die mean value of the parameter X is given by X_d and the location dependent offset values of the parameter X are given by ΔX. The value of the parameter X at any physical point (x, y) in a chip can then be expressed as

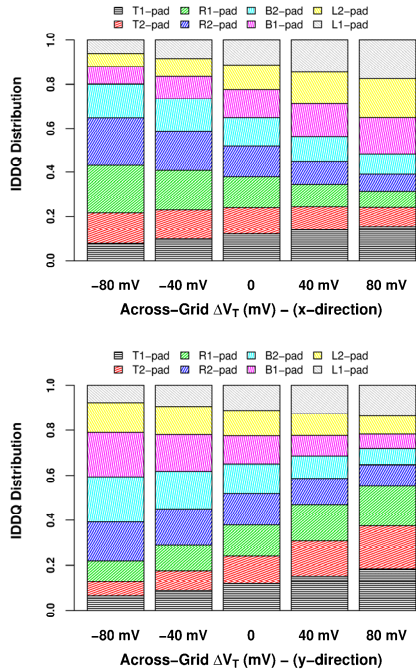$$X(x, y) = X_d + \Delta X(x, y) \qquad (2)$$

Figure 7: Multiple supply port I$_{DDQ}$ ratio signatures for different across-grid variation profiles. The top and bottom set of bars show change in I$_{DDQ}$ ratio signatures for x and y direction across-grid V$_T$ variation, respectively.

The chip mean X_d and the location dependent within-die offset ΔX can take different values for different dies depending on intra-die and inter-die variation. Now let us assume that the within-die variation profile can be represented by a parameterized function f_{wd}. The function f_{wd} can be a simple linear function or it can also include higher-order terms to model any non-linearity present in the within-die variation models. The parameterized function f_{wd} is defined by M number of parameters. The M-dimensional parameter vector **P** can be expressed as

$$\mathbf{P} = \begin{bmatrix} P_1 & P_2 & .... & P_M \end{bmatrix}^T \qquad (3)$$

The within-die variation for a die can be fully characterized if the values of the parameter vector **P** can be obtained for the die. The within-die variation profile is given as

$$\Delta X(x, y) = f_{wd}(\mathbf{P}; x, y) \qquad (4)$$

As discussed in the previous section, the multiple supply port I$_{DDQ}$ signature represents a good estimator of within-die variation. Hence it is possible to extract the within-die variation parameter vector **P** from the multiple port I$_{DDQ}$ ratio signature vector **Q**. The extraction process involves building regression models of within-die variation parameters as a function of the MSP I$_{DDQ}$ ratios using simulation experiments. A linear regression model of the within-die variation parameters in terms of signature vector **Q** is given by

$$\mathbf{P} = \mathbf{A} \cdot \mathbf{Q} + \mathbf{b} \qquad (5)$$

Here A is an $M \times N$ matrix of linear coefficients and **b** is an M-dimensional vector.

The above extraction flow is useful when the models for within-die variation are available. For all practical purposes, the models are usually not well defined and in such cases, it is usually sufficient to compare the MSP I$_{DDQ}$ signature of a die with the base case signature that assumes no across-die variation. The base case MSP I$_{DDQ}$ signature can be obtained through simulation while assuming no

within-die variability. The MSP I$_{DDQ}$ signatures for different chips are routinely measured in an in-line test environment and compared against the base signature to estimate the magnitude and the spatial distribution of within-die variability.

IV. HARDWARE VALIDATION

We validated the proposed multiple supply port I$_{DDQ}$ method through hardware measurements. The measurements were taken on an experimental test-chip fabricated in 65-nm SOI process. In this section, we present the details of the test-chip and demonstrate the sensitivity of the MSP I$_{DDQ}$ signatures to within-die variation profiles.

The focus of this paper is on proving the usefulness of the proposed easurement technique. We do not attempt to report on leakage variations in an actual product. Instead, we introduce leakage variations *artificially* in a small test macro in a controlled fashion to demonstrate the correlation of the MSP I$_{DDQ}$ signature with changes in the leakage distribution characteristics of the macro. The block diagram of the test-chip is shown in Figure 8. The test-chip consists of an array of test circuits as shown in the figure. There are a total of 4000 test-circuits arranged in 80 rows and 50 columns. Each test-circuit in the array comprises of a pseudo test inverter with a PFET and an NFET device connected in series between V$_{DD}$ and G$_{ND}$. The gate terminals of the PFET and the NFET devices in the pseudo inverter are independently controlled through scan flops. The scan flops of all test circuits are connected in a scan chain configuration. The power to the test array is supplied through four power ports located at four corners of the array and labeled as P$_{00}$, P$_{02}$, P$_{10}$ and P$_{12}$ in the figure. Each power port wires out of the chip on a separate pin. The individual current drawn by each of these four power ports can be measured to obtain MSP I$_{DDQ}$ signatures of the test array.
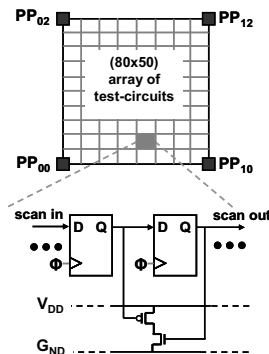

Figure 8: Block diagram of the test macro. The macro contains four power ports labeled as PP$_{00}$, PP$_{02}$, PP$_{10}$ and PP$_{12}$. Schematic of one test-circuit is also shown. The other test circuits are identical.

The instrumentation used for measuring individual power port currents is shown in Figure 9. The setup uses a single external supply and a set of low-resistance mechanical switches, as shown in the figure. The global current source meter represents the voltage source, which also has the ability to measure global chip-wide I$_{DDQ}$. The local current ammeter is configured in series with the switches and the global current source meter to allow measurement of the individual port I$_{DDQ}$s. We use this test setup in our experiments. An alternative production-oriented approach is described in Section V.

The proposed technique is applied during wafer-probe where it is possible to easily access the individual power ports of the die. The biggest challenge in obtaining accurate measurements during wafer probe is dealing with the resistance variations that occur in the power grid, the contactors in the probe card and the external power supply
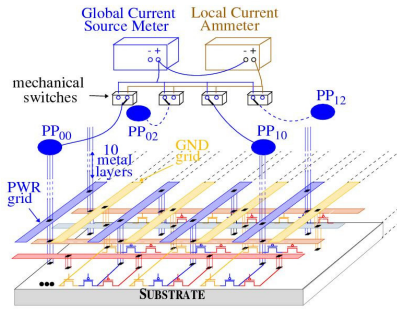
Figure 9: Test instrumentation setup for measuring I_{DDQ} currents through individual power ports.

☐ Inverters in leakage state 1 (both NFET and PFET off)
☐ Inverters in leakage state 2 (PFET off and NFET on)
☐ Alternating inverters in leakage states 1 and 2
☐ Leakage gradient created by varying the number and location of inverters in leakage states 1 and 2
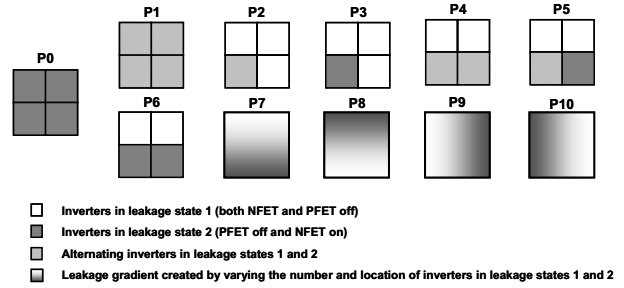
Figure 10: Leakage profiles created in the macro to emulate different within-die variation trends. The leakage profiles were created by controlling the leakage state of the test inverters.

wiring. Resistance variations will introduce changes in the distribution profile of the MSP I_{DDQ} signature that will be indistinguishable from the true I_{DDQ} regional variations that occur on the chip due to within-die variation. In order to eliminate the impact of resistance variations, we use a calibration technique similar to the method proposed in Reference [18].

The calibration technique requires the insertion of a low overhead infrastructure on the chip that consists of a distributed array of stimulus-generating circuits, called calibration circuits, similar in design to test circuit shown in Figure 8. One copy of a calibration circuit is placed under each of the power ports. For the power grid under investigation in this work (see Figure 8), we use the test-circuits under the four power ports as the calibration circuits. A shorting stimulus can be applied to the power grid by enabling both the NFET and PFET devices in the pseudo inverters. The calibration process for a chip involves enabling the calibration circuits, one at a time, and measuring the corresponding shorting currents through each of the power ports. Note that the magnitude of the shorting current created by the calibration circuits is on the order of a couple milliamps, so power grid integrity issues are not a concern. A 2-D array of currents is constructed in this fashion, with rows corresponding to the calibration tests and columns corresponding to the power ports. This matrix is used with the data collected from a corresponding set of calibration tests carried out on a simulation model to define a linear transformation operator X. The matrix X is used to calibrate the measured MSP I_{DDQ} signatures, thereby significantly reducing the impact of resistance variations. Details of the procedure are given in Reference [18].

The area overhead of the calibration infrastructure is very small. For example, the circuit shown in Figure 8, which consists of two FFs and two transistors, can be implemented in 40 um^2 area in a 65 nm process. Assuming 100 copies are inserted in 5 mm x 5 mm chip, the area overhead is less than 0.02%, i.e., (100 x 40 um^2)/25,000,000 um^2 *100. The routing overhead associated with the scan-in, scan-out and scan-clock signals that connect the distributed array of calibration circuits is also small.

We can measure the MSP I_{DDQ} signature of the test macro and extract within-macro variation from the measured data. However, the foot-print of the test macro (558μm x 380μm) is not large enough to observe significant across-macro variation. Hence, in order to validate the correlation between the MSP I_{DDQ} signature and within-die variation, we artificially create different leakage profiles in the macro. The control structure of the test circuit shown in Figure 8 allows us to program leakage currents in different regions of the macro. The leakage of a region can be controlled by varying the input state of the test circuit inverters in the region. If the test inverters in a region are set in the state where both NFET and PFET are off, it emulates the low leakage (and hence higher V_T or higher L_{eff}) region.

Similarly, the leakage of a region can be enhanced by setting the test inverters in the region to the input state where either the NFET or PFET is off while the other device is on. Furthermore, by controlling the number of inverters that are in the high or low leakage state in a region, we can arbitrarily program various across-macro leakage patterns.

Figure 10 shows the set of within-die leakage profiles that were artificially created and analyzed in the experiments. Here leakage state 1 corresponds to the low leakage case where both NFET and PFET devices in the test circuit are off and leakage state 2 represents the high leakage state where only the PFET is off while the NFET is on. The leakage patterns shown in Figure 10 exercise the following configurations:

P0. All test inverters are in the leakage state 2. This state reflects the base state with no within-die variation. The MSP I_{DDQ} signatures of all other patterns are compared against this pattern.

P1. Alternating test inverters are in leakage states 1 and 2. This state also reflects no within-die variation but a lower global I_{DDQ} than the state P0.

P2. Alternating test inverters in the lower left quadrant are in leakage states 1 and 2. The inverters in the remaining three quadrants are in the leakage state 1. This state reflects a within-die trend where lower left quadrant is leakier (faster) than the other regions.

P3. Same as pattern P2 but with all inverters in the lower left quadrant being in the high leakage state 2. This state emulates a scenario where the within-die variation profile is similar to pattern P2 but the magnitude of variation is larger than that in pattern P2.

P4. Alternating test inverters in the lower half are in leakage states 1 and 2. The inverters in the top half are in the leakage state 1, thereby reflecting an across-die trend where lower half is leakier (faster) than the top half.

P5. Same as P4 but with all inverters in the lower right quadrant being in the leakage state 2.

P6. Same as P4 but with all inverters in the lower half being in the leakage state 2.

P7. Gradient with incrementally larger numbers of inverters per row in leakage state 2. For example, top row has no inverters in leakage state 2, second row has 2 inverters in leakage state 2, and bottom row has all inverters in leakage state 2. The pattern creates a downward leakage gradient with the bottom row being leakier than the top row. This pattern may more accurately represent the expected with-in die spatial characteristics in larger chips.

P8. Same as P7 with direction of increasing leakage upward.

P9. Same as P7 with direction of increasing leakage to the right.

P10. Same as P7 with direction of increasing leakage to the left.

We measured the MSP I_{DDQ} signatures for the eleven leakage patterns discussed above. The I_{DDQ} signatures for patterns P1 to P10 were compared against the base case signature of pattern P0. Figure 11 shows the measurement results for one chip. The figure shows the percentage change in the current ratio for the four power ports under different leakage patterns. The percentage change for each port under patterns P1 to P10 is measured relative to the corresponding current for the port in the P0 (reference) case. For example, the percentage change for PP_{00} is calculated as $(I_{pattern} - I_{reference})/I_{reference}*100$. In other words, the bar heights are computed by dividing, port-by-port, the differences in the MSP I_{DDQ} signatures measured under each of the leakage and reference patterns by the MSP I_{DDQ} reference signature and then multiplying each by 100 to express them to a percentage. We refer to the percentage change as a 'ratio'.
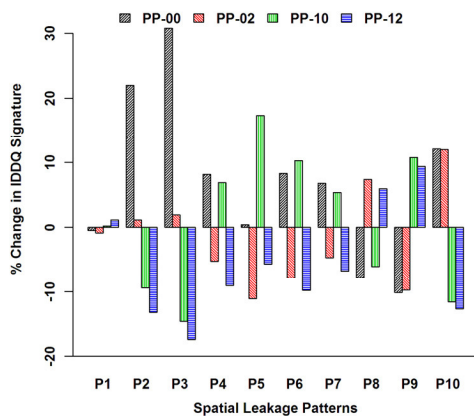

Figure 11: Percentage change in MSP I_{DDQ} signatures for different leakage patterns. The change is measured relative to the pattern P0 with no within-die variation.
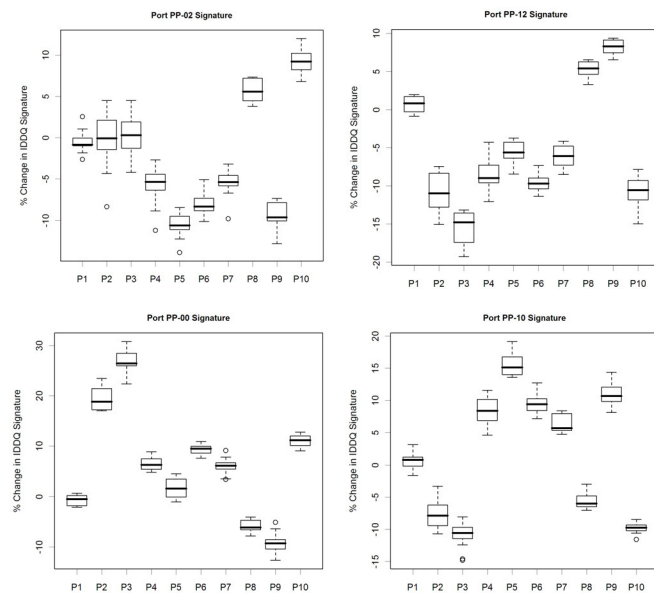

Figure 12: Box-plot of percentage change in the I_{DDQ} ratios of four power supply ports for the leakage patterns shown in Figure 10.

If we compare the results from Figure 11 against the leakage patterns shown in Figure 10, we can see that the two exhibit strong correlation. For example, pattern P1 does not create a within-die variation trend but rather lowers overall global I_{DDQ} for the chip. Therefore, the change in the MSP I_{DDQ} signature for pattern P1 over pattern P0 is almost negligible. On the other hand, patterns P2 and P3 make the lower left quadrant leakier than the other three quadrants. This trend is reflected in the increased current ratio for port PP_{00}, which is in the closest vicinity of the leaky quadrant. The current ratios for other ports are reduced with the largest reduction occurring in the I_{DDQ} ratio of port PP_{12} which is farthest from the lower left quadrant. Furthermore, the percentage increase in the I_{DDQ} ratio of port PP_{00} is larger for pattern P3 than it is for pattern P2. This is true because pattern P3 puts all test inverters in the high leakage state as compared to pattern P2 which only sets alternative inverters in the high leakage state. Similarly, if we look at the measured results for patterns P4 to P6, we see that they all result in an increase in current ratio for ports situated in the lower half of the macro (PP_{00} and PP_{10}). Pattern P4 and pattern P6 exhibit rather symmetric impact on ports PP_{00} and PP_{10}. On the other hand, Pattern P5 causes a relatively larger change in the port PP_{10} ratio than the port PP_{00} ratio due to asymmetric nature of the leakage pattern. The correlation between the region of high leakage and the MSP signatures for gradient leakage patterns P7 through P10 is also very strong. These results indicate that the MSP I_{DDQ} ratios not only track the spatial profile of within-die variation, but the magnitude of the change in the MSP I_{DDQ} signature is also proportional to the degree of within-die variation introduced by the leakage patterns.

The above experiments were carried out on fourteen chips. Figure 12 shows the 'percentage change' metric for the chips in box-plot form in a set of four graphs, one graph for each power port. The box-plot depicts the spread of the ratios across the chips for each leakage pattern. Given the small size of the macro and the fact that the ratios are computed relative to leakage on the same chip, it follows that the variances should be very small. Although a portion of the variance is due to intra-die variation, the main source of the variance is measurement noise. This is most evident in the box-plots for leakage pattern P2 where the majority of the shorting inverters in the array are configured in their low leakage state and therefore, the magnitude of the current measured for this pattern is closer to the noise floor. We computed the noise floor for patterns P2 to be approximately 4%, and the noise floor for the other patterns to be in the range of 1-2%. Setting this aside, the figure clearly shows that the programmed within-die patterns modulate the I_{DDQ} signatures in a fairly consistent manner. These results validate our claim that the MSP I_{DDQ} signature is a reliable indicator of within-die variation.

V. IMPLEMENTATION ISSUES

In order to make the MSP leakage characterization method practical, a technique is needed that is able to measure all the power port currents of the chip without paying a huge penalty in terms of test time. Traditionally, current measurement capabilities of automated test equipment (ATE) were quite limited. However, modern SOC testers have incorporated more enhanced current measurement capabilities. As an example, the V93K SOC tester from Verigy has multiple choices for measuring current. The first option is to use the per-pin parametric unit (PPMU) for measuring multiple supply pad currents. The second and more advanced option is to use a VI32 or a DPS32 card [19]. Each of these cards is equipped with 32 independent channels for sourcing and measuring DC signals with excellent accuracy and throughput. The smallest of the V93K test heads (compact test head) can accommodate a total

of 18 cards where as the larger test heads can accommodate even more. In certain applications, a tester like the V93K may prove to be too expensive for capital investment. In such a scenario, a custom load board or a Wafer Prober Interface (WPI) board will provide a much better cost effective solution. Designing custom load boards for specific applications is routinely done in the ATE industry. The technique presented in the following paragraph focuses on a WPI board custom solution for measuring the MSP I_{DDQ} signatures.

The basic implementation of a WPI board solution is shown in Figure 13. Resistors R_0 through R_m are placed in series with the m power ports labeled PP_0 through PP_m of the IC under test. The measurement circuit comprises of n signal pre-conditioning circuits (IA_V_0 through IA_V_n) followed by n analog-to-digital converters (ADC_0 through ADC_n). Current measurement is accomplished by measuring the voltage differential across the individual resistors R_0 through R_m. In an ideal situation where resources are not significantly constrained, every supply port can have its own ADC sampling circuit. In this scenario, the throughput of the system will be similar to that of a single point IDDQ measurement because all individual power port measurements can be taken simultaneously. Unfortunately, such an ideal scenario is seldom possible. Load boards have a limitation on the available real estate. A lot of PCB space is used up for interfacing pogo cable connections, pogo tower connections and other mechanical features like board stiffeners. Therefore, a more common scenario is that the number of ADCs and associated measurement circuits are less than the number of supply ports to be measured. The switches indicated by 'SW' in the figure route a set of n (out of m where $m > n$) supply ports to the ADCs at any given measurement cycle. Once the measurements of a set of n supply ports are completed, another set of n supply ports are selected by the switches. The switches can be selected from a variety of commercially available integrated solid state types. Since the switches are used for routing voltage signals, the magnitude of the switch on-resistance and the variability in the on-resistance do not impact the measurements. The input impedances of the signal conditioning circuits are much higher than the switch on-resistances and hence the effects of on-resistance can be ignored for all practical purposes. Switch control and ADC data acquisition can be controlled by tester digital resources or by incorporating a microcontroller or FPGA based controller system on the board itself.
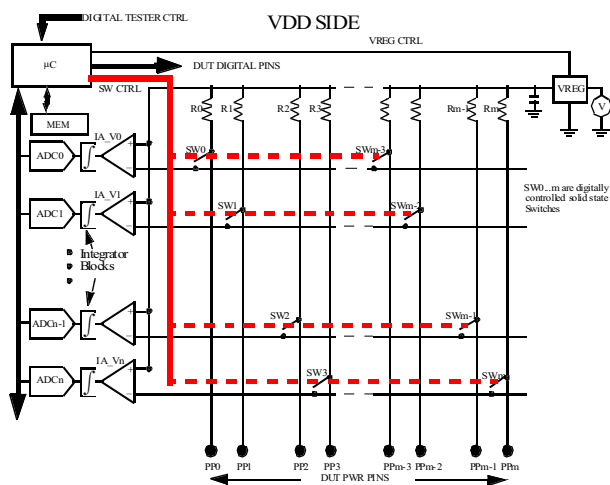

Figure 13: Proposed WPI board instrumentation to measure MSP I_{DDQ} signature for within-die leakage characterization.

VI. CONCLUSION

We proposed a method for monitoring within-die variation using multiple supply port I_{DDQ} measurements. The proposed method has a small design and test cost and provides a unique capability over other existing characterization techniques. Our results show that the multiple supply port I_{DDQ} signature, which is a measure of how overall chip-wide I_{DDQ} is distributed among various power ports, correlates very well with the within-die variation. To address test cost issues, a practical and realistic measurement strategy is proposed for wafer-level testing that is capable of measuring a large number of power port currents simultaneously. Due to its minimally invasive nature and low-overhead, the proposed technique can enable regular monitoring of within-die variability in product chips.

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