Calibrating Power Supply Signal Measurements for Process and Probe Card Variations

Dhruva Acharyya and Jim Plusquellic
Department of CSEE, University of Maryland, Baltimore County.

Abstract

The power supply transient signal (I_{DDT}) methods that we propose for defect detection and localization analyze regional signal variations introduced by defects at a set of the power supply ports on the chip under test (CUT). A significant detractor to the successful application of such methods is dealing with the signal variations introduced by process and probe card parameter variations. In this paper, we describe several calibration techniques designed to reduce the impact of these types of "non-defect" related chip and testing environment variations on the defect detection sensitivity of I_{DDT} testing methods. More specifically, calibration methods are proposed that calibrate for signal variations introduced by performance differences and by changes in the probe card RLC parameters. The calibration methodology is demonstrated through SPICE simulations and in hardware.

1.0 Introduction

Many defect-oriented testing methods can be characterized as "parametric" because their decision criteria are based on the analysis of analog, continuous circuit parameters. For example, delay fault testing attempts to determine that all path delays in the chip-under-test (CUT) are shorter than a designated cycle time. Power supply signal analysis methods, such as quiescent (I_{DDQ}) and transient (I_{DDT}) current analysis, base the pass/fail status of a CUT on whether the measured supply current is above or below a threshold.

The nature of these defect-oriented methods makes it necessary to define a meaningful threshold between good and bad chips that does not erroneously degrade yield or quality. The difficulty of this task is largely determined by the magnitude of several distinct sources of "non-defect" related variations. One major source of variation is that present in the process itself. The consequence of these sources of variations is to create a distribution among the measured parameters of good (and bad) chips. This blurs the distinction between the two classes of chips, often making it impossible to cleanly separate them. This problem is most evident when the tails of the good chip distribution overlap the tails of the bad chip distributions.

Technology trends are increasing the level of variability in many of the chip's tested parameters. The most well known of these is leakage. The first order characterization that is most often cited to describe leakage trends is leakage increases by an order of magnitude per technology generation. An increase in the mean is nearly always accompanied with an increase in variance. These trends increase the difficulty of defining a meaningful threshold that can be applied universally to all CUTs.

Although the trends in process variation make it imperative to perform some form of calibration in many defect-oriented testing methods, this is not the only source of variation that introduces differences in the measured parameters of good chips. Other sources such as those introduced by the actual testing process are often ignored. This paper identifies and analyzes several sources of variations that have an impact on I_{DDT} testing methods and describes calibration techniques designed to enhance the level of transparency to them within the testing process. Although the focus of our work is on I_{DDT}, the techniques described may be useful in the broader context of defect-oriented testing.

The remainder of this paper is organized as follows. Section 2.0 describes related work. Section 3.0 describes the simulation model and method. Section 4.0 describes the calibration procedures. Section 5.0 describes the simulation experiments. Sections 6.0 and 7.0 demonstrates the effectiveness of the calibration methods in simulation and hardware experiments, respectively. Section 8.0 presents our conclusions.

2.0 Background

The trends and predictions given in ITRS for subthreshold and gate leakage currents in current and future technologies threaten the viability of I_{DDQ} testing [1]. Calibration techniques, such as current signatures and ratio-I_{DDQ}, are proposed to reduce the mean and variability of I_{DDQ} in [2][3] and [4]. These techniques rely on a self-relative or differential analysis, in which the average I_{DDQ} of each chip is factored into the pass/fail threshold. A calibration technique based on the analysis of multiple power supply port signals is proposed in [5].

With regard to I_{DDT} methods, calibration methods are proposed in the testing techniques described in [6] and [7]. The experimental results presented in [6] analyze I_{DDT} through V_{DDT} variations in the steady-state signals of primary outputs. Calibration for process variations is performed by computing ratios of the waveform areas of signals measured on different outputs, i.e., at different topological locations on the CUT. Calibration for measurement noise is performed by analyzing waveform differences computed using the waveforms measured at the same test points on different chips. In [7], the ECR method cali-

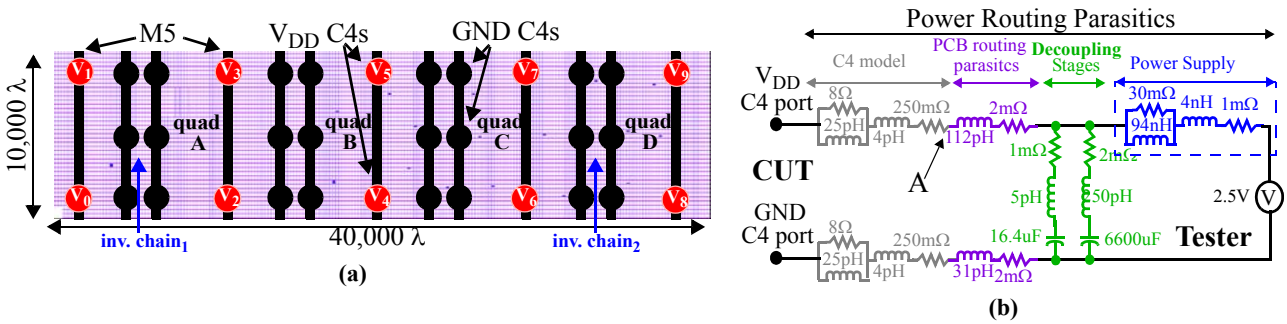

Figure 1. (a) Portion of a commercial power grid called the "Q4" (b) power distribution system model.

brates for process variation by computing ratios from the time domain I_{DDT} waveform areas measured at a signal supply point as different test sequences are applied.

3.0 The Simulation Model and Method

In this section, we describe the important features of the I_{DDT} testing method called Transient Signal Analysis (TSA). The method is described in the context of the simulation model used in the simulation experiments discussed in Section 5.0.

3.1 Simulation Model

A portion of a commercial power grid called the Q4 is shown in Figure 1(a). The Q4 consists of four quads labeled 'quad A' through 'quad D', occupies a 10,000 by 40,000 λ area and interfaces to a set of external power supplies through an area array of 10 V_{DD} and 24 GND C4 pads. A C4 pad is a solder bump for an area array I/O scheme.

The Q4 is constructed over 5 layers of metal, with metal 1 (M1) and metal 3 (M3) running vertically and M2 and M4 running horizontally. The C4s are connected to wide runners of vertical M5 that are in turn connected to the M1-M4 grid. The mesh configuration of the V_{DD} and GND grids are connected together across metal layers with stacked contacts. We derived an RC model of the Q4 using an extraction script that preserves the physical structure of the metal interconnect in the topology of the RC network, i.e. no network reduction heuristics were applied. The resistance per square and the overlap capacitances per unit area of TSMC's 0.25 μm 5 metal process used in the extraction process were obtained from published parameters [8].

The RC model of the Q4 consists of approximately 80,000 resistors and 100,000 capacitors. Another 30,000 capacitors and corresponding equivalent series resistances are distributed uniformly across the layout region to represent the transistor source and on-chip decoupling capacitance. The power distribution system (PDS) model shown in Figure 1(b) was used to represent the tester's power supply, probe card and C4 connections to the chip (see [9] for details). The probe card *PCB routing parasitics* and *C4 model* elements are replicated for each of the V_{DD} and GND C4 ports in the simulation model.

3.2 Power Supply Transient Signal Analysis

The novelty of our method derives from the use of multiple power supply signal measurements. These signals are measured simultaneously as a means of detecting (and locating) the regional signal variations introduced by defects. For example, the transient signals generated at each of the 10 V_{DD} C4s in Figure 1(a) are measured and analyzed, as a test sequence is applied to the primary inputs and/or scan latches of the core logic.

The basic strategy underlying the method is to make use of the spatial variations in the transient signals measured individually at each C4 as a means of detecting the defect. The impedance profile of the power grid and PDS described in [9] suggests that the transient signal variation introduced by the defect will manifest in the surrounding C4s proportional to the "equivalent impedance" between the defect site and each of the C4s. One way to detect the defect is to develop a mapping from the measured supply currents to layout coordinates, as described in the following paragraphs. In this work, the area under the I_{DDT} waveform is used in the analysis procedure. The I_{DDT} waveform areas are subsequently referred to as IAs.

Process variations impact performance and the corresponding magnitude of the measured IAs. Ideally, the layout position predicted by the mapping procedure should be independent of performance variations. This is accomplished by computing **current fractions** using the IAs measured at pairings of C4s. For example, the I_{DDT} current fraction, δ_{01}, defined for a C4 pair labeled V_0 and V_1 in Figure 1(a) is given by Equation 1. This form of calibration is subsequently referred to as **performance calibration** (PC).

$$\delta_{01} = \frac{IA_0}{(IA_0 + IA_1)} \qquad \text{(Eq. 1)}$$

Figure 2 shows the relationship between current fractions and the layout position of a stimulus in the region defined as 'quad A' in Figure 1(a). In each simulation, a tri-

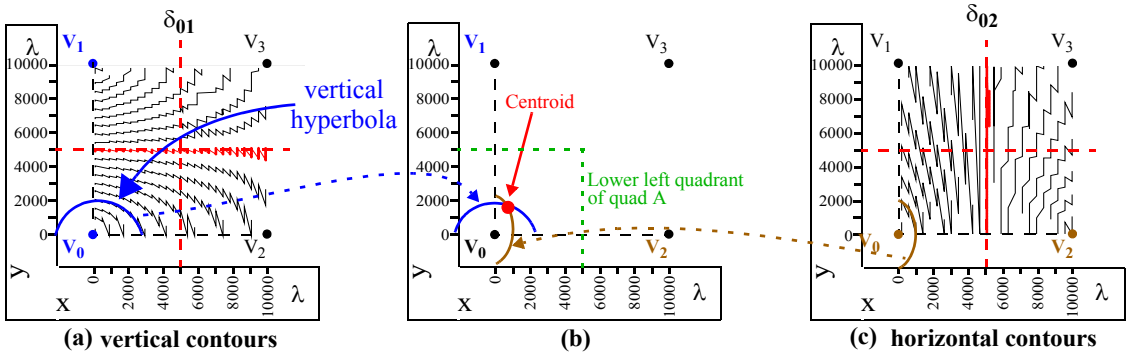

Figure 2. Contour plots of δ_{01} (a), δ_{02} (c) and illustration of mapping procedure (b).

angle wave stimulus, $i_s(t)$, was connected at a unique position between the V_{DD} and GND metal 1 runners in the layout. The simulations were repeated for approximately 3,000 different locations of $i_s(t)$ and the areas under the I_{DDT} waveforms produced through point 'A' in the PDS model of Figure 1(b) were computed for the surrounding C4 pads labeled V_0, V_1 and V_2.

The set of current fractions δ_{01} and δ_{02}, computed over the two dimensional space for C4 pairings V_0-V_1 and V_0-V_2, were sorted to produce the contour plots shown in Figure 2(a) and (c), respectively. A contour is defined as all the (x,y) layout positions for $i_s(t)$ that produce a similar current fraction for a given V_{DD} pairing. These contour curves are well approximated analytically as a *family* of hyperbola curves. Examples of vertical and horizontal hyperbola curves are shown superimposed on contour plots in Figure 2(a) and (c).

Although the details of the hyperbola mapping procedure are given elsewhere [10], the concept is simple. A logic test is applied to the CUT and the IAs are computed from measurements at the C4s. Within each quad, two current fractions are computed using the IAs from two pairings of C4s, and a vertical and horizontal hyperbola are derived, as shown in Figure 2(a) and (c). The intersection of these two hyperbolas defines an (x,y) coordinate that represents the center or *centroid* of transient activity within the quad under the logic test. The same procedure is applied to the other quads of the CUT. The set of centroids for the CUT are then compared with those obtained from known defect-free reference chips (or simulations) under the same logic test. If any of the centroid positions for the CUT is significantly different (in the statistical sense), the CUT is deemed defective.

Since current fractions eliminate performance differences between defect-free chips, the positions of the centroids among the defect-free chips are similar under the test sequence. The presence of a defect, on the other hand, will introduce regional signal variation and will move the centroid in one or more quads, allowing it to be detected. The quads that are most significantly affected are those adjacent to the quad containing the defect because they are positioned to receive a mix of defect and defect-free signal variation. Reference [10] presents the results of a set of simulation experiments that confirm this behavior.

4.0 Calibration Methods

The objective of calibration is two fold: 1) to reduce signal variations that are not of interest, such as those introduced by process variations, and 2) to "calibrate" the measured values such that a universal pass/fail criteria can be applied to the entire set of chips. Current fractions were described in the previous section to accommodate for global performance variations. Unfortunately, current fractions by themselves are not "powerful" enough to accommodate for variations in the testing environment. Here, calibration transistors and a simple linear algebra technique are proposed as a means of calibrating the measured IAs and for providing a common framework for the comparing chip data. More specifically, the procedure is able to calibrate the IA data from a test CUT to a set of values that would have been measured under a different set of probe card parameters.

4.1 Calibration Circuits

The 250 mΩ resistors adjacent to point *A* in Figure 1(b) represent probe contact resistances, and have the potential to vary widely from touch down to touch down of the probe card. Due to the low impedance nature of the power grid, even small changes in contact resistance can introduce large changes in the distribution of the current to the C4s. The calibration procedure described in this paper is capable of virtually eliminating signal variations caused by probe card variations, and is also able to reduce signal variations introduced by changes in the power grid impedance characteristics across CUTs.

One way to account for contact resistance variations is to add circuitry that allows special *calibration tests* to be performed. The **calibration circuit** (CC) used to perform the calibration tests can be very simple. One such imple-

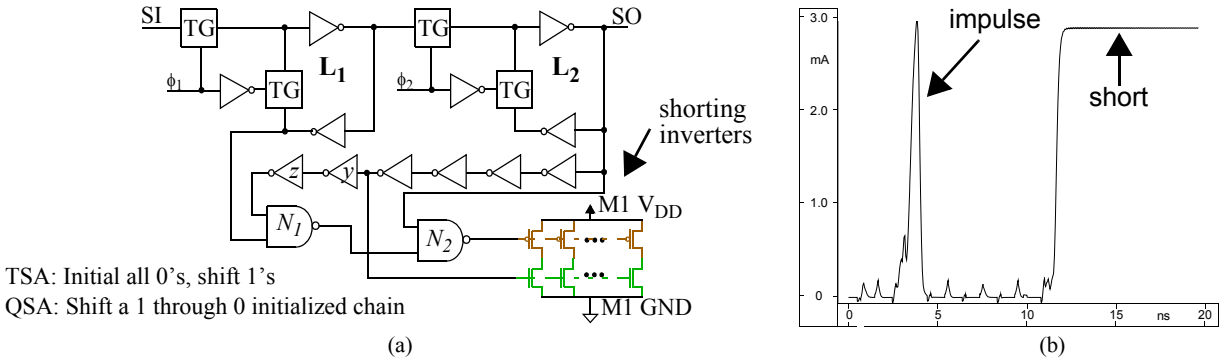

Figure 3. (a) Calibration Circuit (CC) and (b) resulting transient and quiescent current waveforms.

mentation is shown in Figure 3(a), which consists of 2 latches, a delay chain and a set of 'shorting' inverters. The source and drain of the P- and N-channel transistor are connected to the V_{DD} and GND supply grid, respectively, in M1. One copy of this circuit is placed under each of the V_{DD} (and GND) C4s in the CUT.

The latches shown in Figure 3(a) are connected in a scan-chain configuration (and are separate from the scan chains that drive the core logic to enable these tests to be conducted independently). The NAND-NAND (N_1-N_2) logic allows a momentary transient short whose duration is given by the path delay from the input of inverter *y*, through inverter *z* and NAND N_1, to the output of NAND N_2. For example, initializing the scan chain to all 0's and shifting a string of 1's will introduce a momentary short (an impulse) as the leading 1 is clocked into the latch L_2. Similarly, shifting a 1 through a 0 initialized scan chain will generate an edge and then sustain a short for as long as a 0-1 state is kept in L_1 and L_2, respectively. The power supply current waveform that results from these stimuli is shown in Figure 3(b). The features of this waveform indicate that this circuit is able to generate an impulse or an edge for transient signal methods and a steady-state short for quiescent signal methods.

4.2 Calibrating for Contact Resistance Variations

The change in the distribution of current caused by contact resistance variations of the probe card can be calibrated out using a procedure based on linear transformation. In the context of a testing scenario for a commercial chip, the procedure is carried out as follows. After the probe card is seated on the CUT *T*, the CC tests are performed. The calibration procedure uses this CC data and the CC data collected from a reference chip *R* (or simulation model) to compute a transformation matrix *X*. The *X* matrix is then used to translate the currents measured from *T* under a logic test to the currents that would have been measured if *R*'s probe contact resistances were used. In other words, the currents measured from *T* are calibrated to the *R*'s probe card parameters. The transformation procedure is subsequently referred to as **probe card calibration** (PCC).

In the context of our simulation experiments, the CC data for the portion of the power grid defined only by *quad A* in Figure 1(a) consists of 16 IAs, i.e., 4 IAs from each of the 4 CC tests conducted at V_0 through V_3. The IAs define a matrix of values given by *TCI* in Equation 2 with the rows representing the data from each CC test and the columns representing the C4s. The CC data set for the reference CUT is given by *RCI* in Equation 2.

$$\boldsymbol{X} = \boldsymbol{TCI^{-1}} * \boldsymbol{RCI}$$

$$\begin{bmatrix} x_{00} & x_{01} & x_{02} & x_{03} \\ x_{10} & x_{11} & x_{12} & x_{23} \\ x_{20} & x_{21} & x_{22} & x_{23} \\ x_{30} & x_{31} & x_{32} & x_{33} \end{bmatrix} = \begin{bmatrix} t_{00} & t_{01} & t_{02} & t_{03} \\ t_{10} & t_{11} & t_{12} & t_{13} \\ t_{20} & t_{21} & t_{22} & t_{23} \\ t_{30} & t_{31} & t_{32} & t_{33} \end{bmatrix}^{-1} \times \begin{bmatrix} r_{00} & r_{01} & r_{02} & r_{03} \\ r_{10} & r_{11} & r_{12} & r_{13} \\ r_{20} & r_{21} & r_{22} & r_{23} \\ r_{30} & r_{31} & r_{32} & r_{33} \end{bmatrix}$$

(Eq. 2)

The P- and N-channel transistors in the calibration circuits of the test CUT and reference CUT are not identical because of inter- and intra-die process variations and therefore, the sum of the IAs computed across each row of the *TCI* and *RCI* matrices are likely to vary. In order to eliminate the dependency of the transformation matrix on the CC stimuli, the *TCI* and *RCI* matrix elements are *normalized* by dividing each element by the total current of its respective row.

Equation 2 indicates that the transformation matrix *X* is obtained for the test CUT *T* by computing the matrix product of TCI^{-1} and *RCI*. Once *X* is obtained, Equation 3 is used to calibrate the areas obtained under a logic test *n*, T_n, by computing the product of T_n and *X*. The column vector C_n represents the calibrated IAs at each of the C4s, whose values are subsequently used in the current fractions for performance calibration, i.e., to compute δ_{01} in Equation 1.

$$C_n = T_n * X$$

$$\begin{bmatrix} c_0 \\ c_1 \\ c_2 \\ c_3 \end{bmatrix} = \begin{bmatrix} t_0 & t_1 & t_2 & t_3 \end{bmatrix} \times \begin{bmatrix} x_{00} & x_{01} & x_{02} & x_{03} \\ x_{10} & x_{11} & x_{12} & x_{23} \\ x_{20} & x_{21} & x_{22} & x_{23} \\ x_{30} & x_{31} & x_{32} & x_{33} \end{bmatrix} \quad \text{(Eq. 3)}$$

5.0 Simulation Experiments

The PCC and PC procedures are demonstrated using the data from simulations of the Q4 RC model and PDS shown in Figure 1. The positions labeled "inv. $chain_1$" and "inv. $chain_2$" in quads A and D identify the position of the core logic in these simulations. The inverter chains are composed of a sequence of 10 inverters with fan-out (not shown). Although the core logic is extremely simple, it serves to demonstrate the nature of the transformations performed by PC and PCC.

Eight sets of TSMC's 0.25µm process parameters were used to create 8 RC models of the power grid and 8 RC-transistor models of the inverter chains [8]. The inverter chains were simulated under the 8 process models to obtain the I_{DDT} waveforms. Piece-wise linear fits to the I_{DDT} waveforms were used to configure two SPICE current sources that were connected between M1 V_{DD} and GND runners at the positions labeled as "inv. $chain_x$" in Figure 1(a). The 8 pairs of I_{DDT} waveforms were used as the stimulus in a sequence of SPICE simulations of the Q4 RC and PDS models. Under each simulation, a set of 10 IAs were computed from the I_{DDT} waveforms generated at the 10 V_{DD} C4s in Figure 1(a), labeled V_0 through V_9. Therefore, 8 sets of 10 IAs were used as the input to the PC and PCC procedures.

In addition to the logic simulations, a set of 10 CC simulations were also performed for each process model. The same procedure was followed, i.e., the calibration test layouts were extracted and simulated. The piece-wise linear fits to the I_{DDT} waveforms were used as the stimulus to drive the grid at the C4s. Since there are 10 V_{DD} C4s, the simulations were repeated 10 times with each stimulus under each process model. Therefore, 8 sets of 100 IAs were used as the calibration data for the PC and PCC procedures.

In order to determine the effectiveness of the two calibration procedures, PC and PCC, the logic and calibration test simulations were performed under 4 different test configurations. Two of the four test configurations used a single Q4 RC model in all simulations along with two distinct PDS models. For the base configuration, the power grid obtained from TSMC model *t08p* was used (see [8]) in combination with a set of uniform *Probe card* and *C4* models, e.g., 250 mΩ was used as the contact resistance for all C4 connections. In the second configuration, each of the contact resistances for the 10 V_{DD} and 24 GND C4s was randomly varied between 250 mΩ and 750 mΩs. These two configurations are labeled *CP-CG*[1] and *VP-CG* for constant and variable probe card (CP & VP) and constant grid (CG). In the remaining two test configurations, the 8 power grid RC models were used in the simulations under the two PDS models. The models are labeled *CP-VG* and *VP-VG*. Under these guidelines, the *VP-VG* simulations most closely represent an actual test environment in which it is expected that power grid RC parameters vary from chip-to-chip and the probe card contact resistances vary from C4-to-C4.

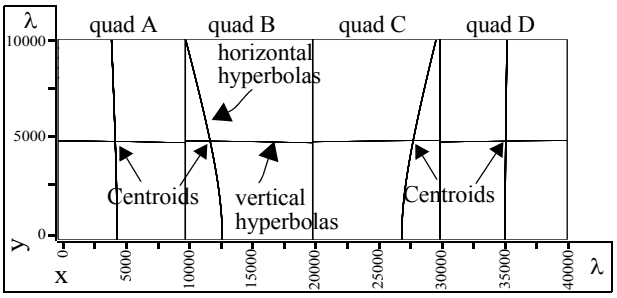

Figure 4. Hyperbolas obtained from 8 process models under *CP-CG* test configuration.

The procedure described for PCC in the previous section used, as its example, the CC test data from quad A only. In this analysis, the simulations of the Q4 generate a matrix of 100 values and therefore, the matrix and vector elements shown in Equations 2 and 3 are 10x10 and 1x10, respectively.

The CC test data used to represent reference CUT *R* (matrix *R* in Equation 2) was obtained from the *t08p* power grid and uniform PDS model simulation associated with the *CP-CG* test configuration. The CC test data from each of the 8 test CUTs is used as the elements of matrix *TCI* in Equation 2 to derive a transformation matrix *X*. As noted above, the IAs in the *TCI* and *RCI* matrices are normalized in the matrix by dividing all elements in each row by the sum of the IAs in each row. This operation serves to null out performance variations in the calibration circuits themselves between (and within) CUTs, and allows the *X* matrix to solely represent the transformation from one set of probe card (and power grid) parameters to another.

In our experiments, there are 8 sets of CC test data corresponding to the 8 RC-transistor models of the calibration circuit and power grid, including the reference. Therefore, 8 *X* matrices are computed in each of the four test configu-

1. *C* for constant
   V for variable
   P for probe card model
   G for grid model

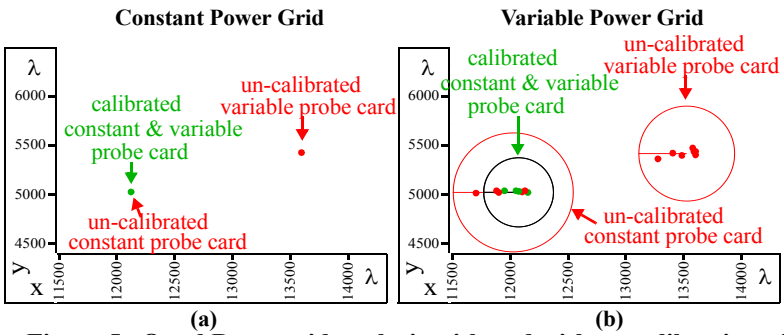

Figure 5. Quad B centroid analysis with and without calibration of data from 4 sets of probe card and power grid simulation models.

Sim. Model	un-calibrated data (λ)		calibrated (λ)	
	(x, y) (λ)	**3 σ**	**(x, y)**	**3 σ**
CP-CG	(12103, 5019)	1.3	(12103, 5019)	1.9
VP-CG	(**13554**, **5363**)	4.4	(**12104**, **5018**)	4.0
CP-VG	(12004, 5018)	509	(12049, 5019)	297
VP-VG	(13477, 5350)	407	(12050, 5018)	295

Table 1: Centroid statistics from Figure 5.

rations. However, the 8 *X* matrices computed under the CP-CG test configuration are the identity matrix because of the absence of power grid and probe card variations.

6.0 Simulation Results

Performance calibration using current fractions is designed to reduce the impact of global process variations on the sensitivity of the defect detection procedure. The hyperbola curves shown in Figure 4 illustrate the results of applying the TSA detection procedure to the data obtained under the base test configuration, *CP-CG*. Here, the only source of signal variation is from the performance differences in the simulated inverter chains under the 8 process models. For each simulation, TSA uses the computed current fractions to derive 4 sets of vertical and horizontal hyperbolas, one pair for each quad. Although it is not evident in the figure, each "centroid" (defined as the intersection of a vertical and horizontal hyperbola) is actually composed of 8 centroids. It is clear from these results that PC is effective at eliminating performance differences in the inverter chains under the various process models.

The PCC process is designed to calibrate data as a means of establishing a common centroid for all defect-free chips tested under a logic test. The results of applying the TSA detection procedure to the 4 sets of simulation data with and without first applying PCC are shown in Figures 5(a) and (b) for quad B. Note that the figures show only a portion of the region defined as quad B. The hyperbolas that define the centroids have been eliminated and 3 σ circles are given to illustrate the dispersion among the centroids under the 8 process model simulations.

Figure 5(a) shows the analysis for the 2 *constant power grid* data sets while Figure 5(b) gives the analysis for the 2 *variable power grid* data sets. Each plot contains 4 data sets with each data set consisting of 8 intersections and a 3 σ circle. The 2 data sets computed without applying PCC are labeled "un-calibrated" in the plots. The procedure used to compute the "un-calibrated" hyperbolas and their intersections uses the original IA vectors T_n while the "calibrated" uses the calibrated IA vectors C_n.

The positions of the centroids from the 4 data sets in Figure 5(a) are nearly identical and the 3 σ limits are very small, with or without PCC. However, the 8 centroids for the un-calibrated *VP-CG* test configuration are translated up and to the right by approximately 1,500 λ. Table 1 gives the un-calibrated and calibrated "mean" centroid positions and 3 σ statistics (column pairs) for the 4 types of simulation models (rows). The mean centroid position given in the 2nd row, 2nd column (*VP-CG*) illustrates the impact of the non-uniform contact resistance without PCC. In contrast, the calibrated mean centroid position (2nd row, 4th column) is nearly identical to the 2 means given in the first row. The 3 σ statistics for the *VP-CG* data (2nd row) are larger than those given for the *CP-CG* data (1st row) but these increases are very small relative to the dimensions of the quad (10,000 λ x 10,000 λ).

The data sets shown Figure 5(b) illustrate the impact of variations in the RC parameters of the Q4. The patterns in the positions of the centroids in both Figures 5(a) and (b) are similar. However, the dispersion of the data points increases significantly in the *variable power grid* results (note the scales of both plots in (a) and (b) are identical). For example, the un-calibrated *CP-VG* 3 σ value increases from 1.3 λ for the *CP-CG* to 509 λ (see Table 1). An increase in dispersion also occurs in the calibrated data sets of rows 3 and 4 of the table. However, the increase in the 3 σ statistic is smaller, e.g. < 300 λ, which indicates that PCC reduces some of the power grid variation. More importantly, the nearly identical values for the pairs of mean centroid positions and the 3 σ statistics among the calibrated data sets indicates that the PCC remains effective at removing the probe card variations in the presence of power grid variations.

These results illustrate that the PCC procedure is able to meaningfully transform the measured IAs and provide a common frame of reference for comparison of IA data across chips. This is an important feature for improving the level of sensitivity of TSA to signal variations introduced by defects. The regions within the 3 σ circles in the plots of Figure 5 represent the space of defect-free devices. PCC

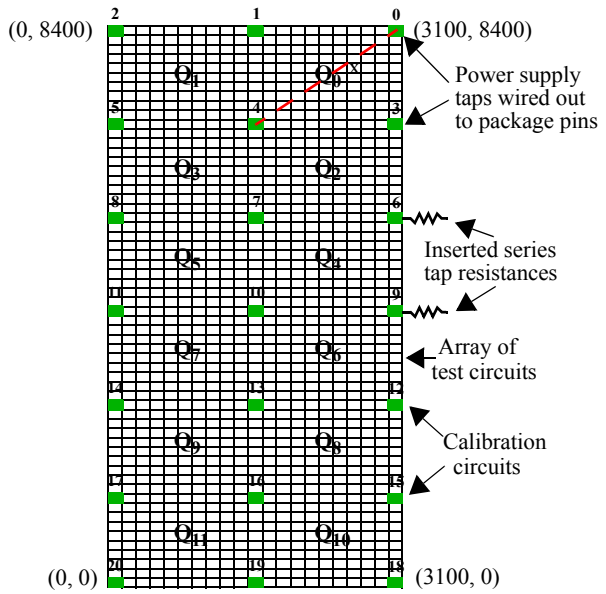

Figure 6. Block diagram of hardware CUT.

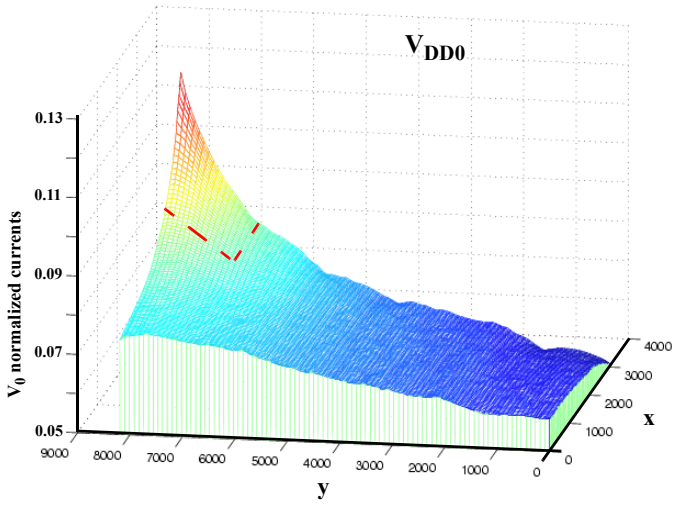

Figure 7. V_{DD0} current profile.

defines a common center and reduces the diameters of these regions without affecting the magnitude of regional signal variation introduced by defects. Reference [10] presents simulation results that illustrate the improvements in detection sensitivity provided by PCC.

7.0 Hardware Results

A block diagram of the hardware CUT investigated in this work is shown in Figure 6. It consists of a two-dimensional array of test circuits. Each test circuit can be individually enabled to provide a test stimulus to the power grid, by itself or in combinations with other test circuits in the array. The power grid is wired in two metal layers. A set of 21 power supply taps, labeled 0 to 20 in Figure 6, emulate the multiple connection points of a typical power grid in a commercial design. These taps will subsequently be referred to as V_x where *x* represents one of the tap connections.

Quads are identified as regions surrounded by 4 V_x tap points, labeled Q_0 through Q_{11} in Figure 6. Each Quad has a total of 121 test circuits (with the exception of Q_{10} and Q_{11} which have one less row.) The test circuits used to represent the calibration circuits are positioned underneath the V_{DD} tap points.

We emulated R_p variations in the packaged chips by inserting an on-chip resistance in series between the 21 V_{DD} tap points shown in Figure 6 and the C4s (not shown). Examples of these resistances are shown for tap points 6 and 9 on the right side of the figure. The resistances were varied between 1 Ω and 100 Ω to emulate worst case conditions (target values of R_p for probing power ports are usually less than 250 mΩ). Minimum size wires of various lengths were used to implement the resistances.

Keithley 2400 source meters were used to measure the currents on the hardware CUT both globally and locally at the package pins through a bank of hardware switches. A PIC microcontroller allowed the switches to be configured automatically using National Instruments software. The leakage currents were subtracted from each of the measured currents.

The V_{DD} tap currents were measured for the CUT as each of the 1260 test circuits were enabled one at a time. Figure 7 shows the current profile plot for the measurements made at V_0 tap point. The x and y axis in Figure 7 represent the location of the test circuit and the z-axis represents the normalized current drawn through V_0. It is evident from this plot that test circuits in the vicinity of V_0 draw a higher proportion of current from V_0 than the test sites farther away. The shape of the surface reflects the impact of power grid's resistive components on the magnitude of the current sourced through this V_{DD} tap point.

In order to illustrate the distortion introduced by the series tap resistances, it is necessary to compare currents measured at different V_{DD} tap points. This is portrayed in Figure 8(a), which plots the coordinates of the test circuits on the x- and y-axis and the normalized current magnitude on the z-axis. The plot shows a mosaic of *cut and pasted* currents from the individual current profiles of the 21 tap points, such as the profile shown for V_0 in Figure 7. The portion *cut* from the individual plots are those currents generated from test circuits in the vicinity of each tap point. For example, the dotted line in Figure 7 identifies the por-

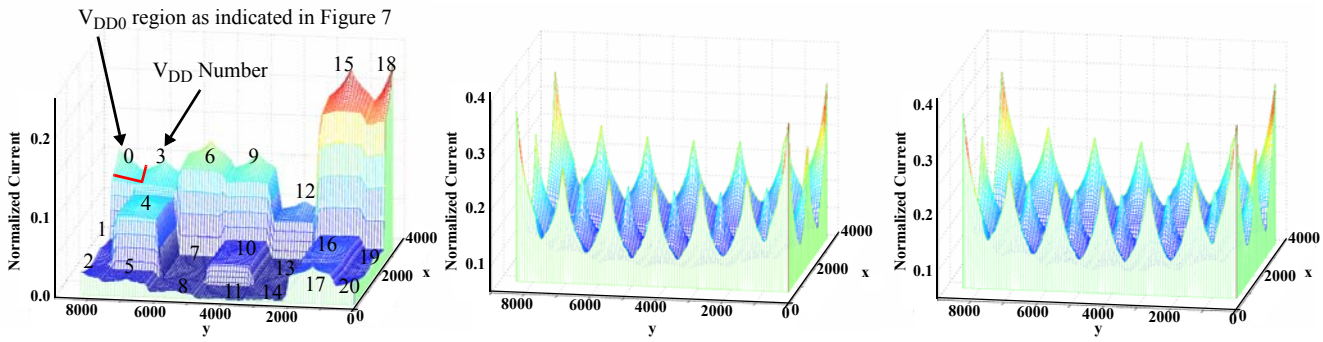

Figure 8. Current profile for (a) un-calibrated hardware (b) simulation (c) calibrated hardware

tion *cut* and then *pasted* into the upper left hand corner of Figure 8(a). A similar operation was performed using the current plots of the other tap points for different regions of the (x,y) space. The numbers in Figure 8(a) indicate the tap point from which the current measurements were made. It is clear from this plot that the large variations in series tap resistances cause the fraction of total current drawn through each of the supply ports to vary widely. For example, peak values range from 0.87% (for V_7) to about 24.04% (for V_{18})

In contrast, Figure 8(b) shows the current profiles under a uniform 1 Ω series tap resistance model, portrayed using the same format as that shown in Figure 8(a). Here, the currents were generated from simulations of a resistance model of the two metal layer power grid used in the hardware CUT shown in Figure 6. A set of 1260 simulations were run on the grid by placing a current source at each of the (x,y) locations corresponding to the positions of the test circuits on the CUT. The uniform series tap resistance eliminates the *distortion* in the distribution of currents to the tap points. The peak currents range from 20.39% (for V_{10}) to 38.04% (for V_2). The larger peaks on the periphery are caused by the non-symmetric distribution of V_{DD} tap points in these regions.

The test circuit currents shown in Figure 8(a) can be calibrated as described in Section 4.2 using the CC data from the hardware CUT and simulation experiments. The result of applying the PCC to the currents shown in Figure 8(a) is shown in Figure 8(c). It is clear that the calibrated hardware data in Figure 8(c) is very similar to the simulation data in Figure 8(b). Thus the calibration procedure has successfully removed the wide variations introduced by the non-uniform series tap resistances.

8.0 Conclusions

Power supply signal analysis methods are promising defect-oriented testing methods for detecting resistive open and shorting defects in advanced technologies. However, the effectiveness of such techniques diminishes as the level of variability in chip parameters increase. Therefore, in order to preserve (and enhance) the sensitivity of these methods to defects, they must incorporate a mechanism to calibrate for "non-defect" related sources of signal variations, such as those introduced by process. The sensitivity of these methods can be further improved if calibration for testing environment variations is also performed. This paper proposes several calibration strategies designed for these purposes.

9.0 References

[1] ITRS (http://public.itrs.net/)

[2] A.E.Gattiker and W.Maly, "Current Signatures", VTS, 1996, pp.112-117.

[3] C. Thibeault, "On the Comparison of Delta IDDQ and IDDQ Test", VTS, 1999, pp. 143-150.

[4] P. Maxwell, P. O'Neill, R. Aitken, R. Dudley, N. Jaarsma, M. Quach and D. Wiseman, "Current Ratios: A self-Scaling Technique for Production IDDQ Testing", ITC, 1999, pp.738-746.

[5] C. Patel, E. Staroswiecki, S. Pawar, D. Acharyya, and J. Plusquellic, "Diagnosis using Quiescent Signal Analysis on a Commercial Power Grid", ISTFA, 2002, pp. 713-722.

[6] J. Plusquellic, D. M. Chiarulli, and S. P. Levitan. "Identification of Defective CMOS Devices using Correlation and Regression Analysis of Frequency Domain Transient Signal Data", ITC, 1997, pp. 40-49.

[7] B. Vinnakota, W. Jiang and D. Sun, "Process-Tolerant Test with Energy Consumption Ratio", ITC, 1998, pp. 1027-1036.

[8] MOSIS process specifications for TSMC's 0.25um process obtained from http://www.mosis.edu/Technical/Testdata/tsmc-025-prm.html

[9] D. Acharyya and J. Plusquellic, "Impedance Profile of a Commercial Power Grid and Test System", ITC, 2003, pp. 709-718.

[10] J. Plusquellic, D. Acharyya, D. Phatak and A. Singh, "I_{DDT}-based Fault Detection and Localization", Submitted to *TODAES*, September, 2003 (http://www.csee.umbc.edu/~plusquel/pubs/todaes_tsa_detect_locate.pdf).