Path Delay Estimation using Power Supply Transient Signals: A Comparative Study using Fourier and Wavelet Analysis

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Abstract

Transient Signal Analysis (TSA) is a parametric device testing technique based on the analysis of dynamic (transient) current (i_{DDT}) drawn by the core logic from the power supply pads in a CMOS digital circuit. In previous work, we develop a test procedure that can be used both to detect signal variations caused by defects and to obtain delay information in defect free chips. Phase spectra of transient signals obtained using discrete Fourier transform are shown to track path delays of defect-free chips under a wide range of process variations. However, in recent work, we were able to demonstrate through simulation experiments incorporating deep submicron transistor models, a circuit design and path sensitization scenario in which our existing TSA method is not able to yield accurate predictions of path delays. More specifically, a circuit composed of two inverter chains constructed with widely varying transistor sizes was shown to produce path delays that were weakly correlated across a set of worst case process models. In this paper, an alternative wavelet-based analysis of i_{DDT} waveforms is shown to improve the accuracy of predicting multiple path delays under these conditions.

Abbreviations:

i_{DDT}: A time varying (ac) signal representing the dynamic current sourced by set of connected gates (path) under an input transition.

1 Introduction

The unique attribute of power supply transient (i_{DDT}) signals to capture the parametric characteristics of the underlying logic circuit enables the development of alternative defect-oriented testing methods. The most important information contained in the i_{DDT} signals is the functional and delay characteristics of sensitized logic paths. The use of power supply transient signals as a means of estimating path delay characteristics has several advantages. First, these signals can be used to detect delay faults introduced by resistive shorting and open defects that are traditionally not targeted by stuck fault based methods. Second, the global observability provided by the power supply transient signals permits delay to be estimated without the need to sensitize paths to observation points such as primary outputs or scan-latches. Third, the supply transients potentially provide a rich source of parametric information about the chip.

Transient Signal Analysis (TSA) is a defect oriented testing technique that exploits the device information contained in the power supply transient signals. Defect detection is accomplished by analyzing the i_{DDT}s measured simultaneously at multiple power supply ports (Pads) on a chip. Linear regression analysis is applied to time and frequency domain representation of the i_{DDT}s to detect outliers [1][2]. Fourier phase analysis of the i_{DDT}s provides a means of estimating path delays in defect-free chips [3].

In recent work, the TSA technique was evaluated under deep submicron process conditions using a circuit design that incorporates gates with widely varying transistor sizes (W/L ratios) [4]. It was discovered that deep submicron variations in process parameters weaken the correlation of delay across logic paths on the same chip. Given the relationship between the delay characteristics of a logic path and i_{DDT} is cause-effect, the reduction in path correlation on the same chip reduces the correlation of i_{DDT}s across chips. Since our delay prediction strategy is based on correlation analysis of i_{DDT}s across chips, it is not able to accurately track all path delays under test sequences that sensitize multiple paths. The limitation of our Fourier phase-based method derives from its focus on the analysis of a single attribute of the i_{DDT} waveform -- its width. However, embedded within the i_{DDT} waveform are other features that can be analyzed as a means of improving the accuracy of predicting multiple independent path delays. The additional dimension of signal decomposition provided by the wavelet transform makes it better suited than the Fourier transform for the extraction and processing of these alternative i_{DDT} waveform features.

In this paper, a set of circuit models incorporating deep submicron process variations and widely varying transistor sizes are simulated to demonstrate the limitations of Fourier analysis for estimating multiple path delays. A wavelet-based analysis is shown to overcome these limitations by providing an extra dimension of "time based" information. The objective of this paper is to compare the computational complexity and accuracy of delay estimation methods based on a discrete Fourier transform (DFT) and a wavelet transform (WT).

The rest of this paper is organized as follows. Section 2 describes related work. Section 3 presents details of the simulation experiments. Section 4 evaluates the characteristics of the i_{DDT} signals under various process models and defines the problem. Sections 5 and 6 describe the path delay estimation procedures and results using Fourier and wavelet analysis, respectively. Section 7 analyzes the computational complexity of the two approaches. Section 8 presents our conclusions.

2 Background

The literature contains a wide range of publications on the application of wavelet transform ranging from seismic and biomedical image processing to electronics. Papers related to the latter topic include the following. Santoso el al. [5][6] applied the WT to detect and localize disturbances in electric power lines. Since electric power signals are ideally composed of a single frequency component, any anomaly in these signals can be detected by analyzing the high frequency (details) components of the WT representation. Bhunia et al. [7] applied the WT on power supply transient signals to detect short and open defects. The mean square differences between WT coefficients of a golden chip and

that of the test chip are used to identify defective chips. Defect localization is achieved by mapping the time at which the WT coefficient of the defective chip differs from that of the defect-free chip into logic depth.

3 Simulation Experiment Design

Figure 1 shows the layout of the test circuit used in the simulation experiments. The layout consists of two paths implemented using chains of inverters. The heads of the two paths are labeled "Fast Path Input" and "Slow Path Input" in Figure 1. The fast path is composed of transistors with W/L ratios ranging from 2 to 5 for n-MOS and 4 to 10 for p-MOS while the slow path is composed of minimum sized transistors with W/L ratios of 1.5. The inverters along both paths fanout to as many as three other inverters in addition to the next inverter in the path. The purpose of using various transistor sizes and loading conditions is to introduce diversity in the i_{DDT}.

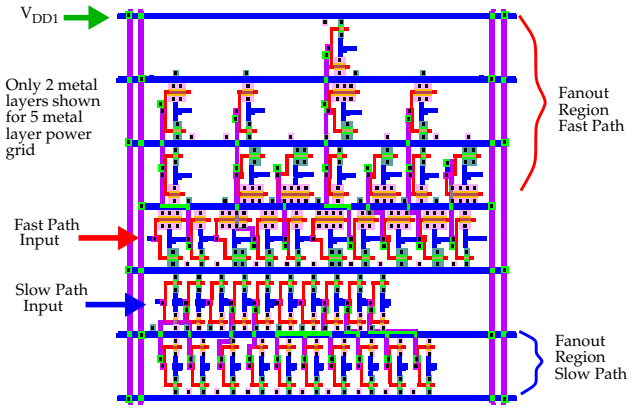

Fig. 1. Layout incorporating dual paths of 10 inverters with a fast path (upper) and slow path (lower)

The supply grid in this design is routed in 5 metal layers (the figure shows only the lower metal 1 and metal 2 layers for clarity). The SPICE voltage source representing the power supply is connected to metal 5 at the point shown on the upper left of Figure 1.

The process models are derived from a set of MOSIS specifications for TSMC's 0.25µm process [8]. Each of the specifications include lot-averaged conductor RC parasitics and BSIM modeling parameters derived from test structure measurements. We had 14 such data sets available. These data sets were used to configure a set of technology files for the SPACE extraction tool [9] and the corresponding SPICE simulation models were extracted from the layout. These parameter values represent worst case values because they were obtained from wafer lots fabricated over a period of several years.

The test stimulus drives both paths simultaneously, as a means of representing the more common multi-path signal propagation model. Since the supply grid is unified, the i_{DS} signals generated by the inverters along both paths superimpose in a composite-i_{DDT} curve. Figure 2 shows a simplified logic level representation of the inverter chains (without the fanout branches). The i_{DS} curves shown beside each inverter represents the spatial distribution of transient current drawn by the corresponding inverter from the V_{DD} rail. The curves labeled i_{DDTfp} and i_{DDTsp} represent the current transients generated by fast and slow paths respectively, when these paths are sensitized separately. The curve labeled i_{DDT} on the right is the waveform that is generated when both paths are sensitized simultaneously.

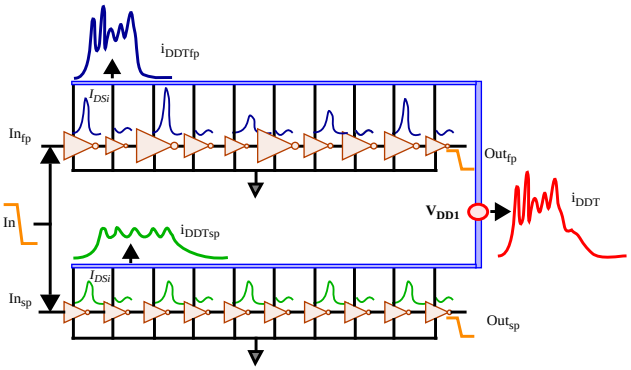

Fig. 2. Illustration of composite-i_{DDT} formation from individual gate i_{DS} curves.

4 Multiple Path Sensitization Challenges

In order to determine the relationship between path delays and the corresponding i_{DDT}s under the different process models, it is first necessary to evaluate the signal propagation characteristics along each of the two paths across the process models. Figure 3 shows the output waveforms from the last inverters of the two paths superimposed in each row. One pairing is shown for each of the 14 process models. Even though the transistor models are identical for all transistors in each circuit model, it is clear across many of these pairings that the delays between the fast and slow paths are not well correlated. (The vertical dotted line provides a reference point for comparison.) This is particularly noticeable for the pairings labeled *h*, *j* and *l*. Here, significant speed-up is observed in the fast path delay while the slow path delay remains relatively constant and consistent with other slow path delays from other runs, e.g., *g*.

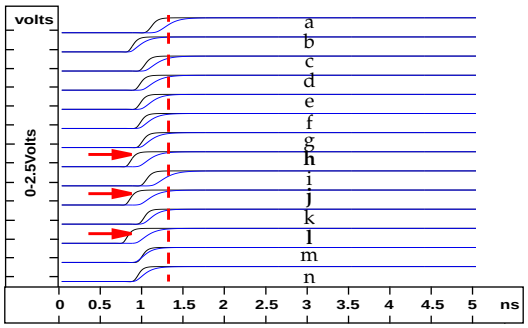

Fig. 3. Path outputs under 14 TSMC's process models with varying BSIM parameters.

The low level of correlation in the delays across the output waveform pairings is largely due to the V_t dependency on transistor width (W) in the BSIM modeling equations. The variations in other "passive" elements of the simulation models have only a small impact on the delay characteristics, as illustrated below.

Figure 4 plots the relative delays of the slow path versus the fast path. The relative delays are computed by subtracting the absolute slow and fast path delays under each of the models from the corresponding absolute path delays of first (and slowest) process model, *a* (given at (0,0) in the figure). It is clear in Figure 4 that correlations between the two paths across the process models is poor. For example, the data points spanning the region labeled "Actual BSIM Parameters" are poorly approximated by a straight line. In contrast, the data points spanning the region labeled "Constant BSIM Parameters" are the relative delays obtained when the

"actual" BSIM models are replaced with the BSIM model from process *a*. These data points span a much smaller region and are nearly co-linear.

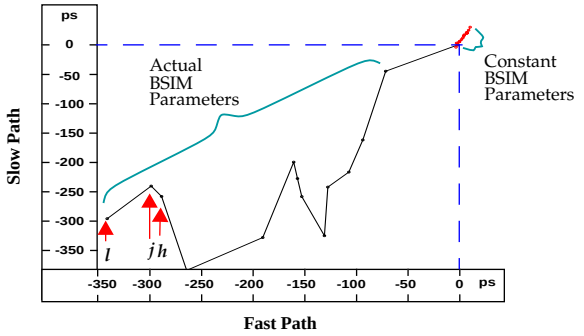

Fig. 4. Slow path vs. fast path relative delays.

Since our method analyzes i_{DDT} as a means of predicting delay, it is important to understand how "weakly correlated" multiple path delays affect the i_{DDT} features. The waveforms labeled i_{DDTfp} and i_{DDTsp} in Figure 5 represent the transient signals generated under single path sensitization using process model *i*. The top-most signal represents the composite-i_{DDT} generated under dual path sensitization. The i_{DDTsp} waveform has a larger width but is smaller in amplitude in comparison to the i_{DDTfp} waveform. This results from the smaller W/L ratio used for the transistors in the gates of this path.

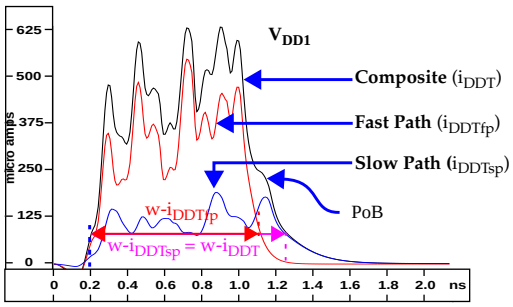

Fig. 5. i_{DDT} waveforms of fast and slow path (bottom) and the composite (top)

The width of i_{DDTsp}, denoted by w-i_{DDTsp} in Figure 5, is similar to the composite width w-i_{DDT}. (The widths are shown measured above the zero baseline in the figure). This indicates that the width of the composite-i_{DDT} is defined by the slow path delay. However, the larger amplitude i_{DDTfp} introduces a sharp change in the composite-i_{DDT} on its falling transition. The i_{DDTfp} also decays before the i_{DDTsp} and leaves a "Posterior-Bump" (or PoB) in the composite-i_{DDT}. The time of occurrence of the PoB coincides with the end of i_{DDTfp} and is a feature that can be used to obtain w-i_{DDTfp}.

The above analysis suggests that a time domain analysis of the composite-i_{DDT} is sufficient to estimate both w-i_{DDTfp} and w-i_{DDTsp}, and the corresponding fast and slow path delays. However, the environmental noise (and EMI) and the parasitics present in a production test equipment make it difficult to obtain the i_{DDT} waveform in its pure, core logic generated form. The ability to select and analyze specific frequency bands using the frequency domain representation of i_{DDT} makes it attractive as a means of overcoming the test environment limitations.

5 Path Delay Estimation using Fourier Analysis

The Fourier transform decomposes a signal into a linear sum of sinusoids or cosinusoids with different frequencies. Eq. 1 gives the expression for a discrete Fourier transform (DFT) of a signal x(t). Here ω and t are discrete variables that represent frequency and time respectively.

$$X(\omega) = \frac{1}{N}\sum_{t=0}^{\frac{N}{2}} x(t)e^{-\frac{j2\pi tk}{N}} \qquad \textbf{Eq. 1.}$$

where k denotes a discrete frequency [k=0,1,2.....N/2]
and t denotes a discrete time sample [t=0,1,2.....N-1]

We have observed that process variations introduce two main types of variations in the i_{DDT} signal, shift and scaling. The Fourier phase component of the frequency domain representation of i_{DDT} naturally tracks time shift and scaling and is therefore the basis of our delay estimation technique.

The Fourier shift property states that a *time shift* (delay) of *d* units causes a phase shift of ω**d* in the frequency domain. This property is expressed formally by Eq. 2 for a signal x(t) with the

$$x(t) \Leftrightarrow X(\omega) \quad \text{or} \quad x(t) \Leftrightarrow M(\omega)\angle\theta(\omega) \qquad \textbf{Eq. 2.}$$
$$x(t-d) \Leftrightarrow X(\omega)e^{-j\omega d} \text{ or } x(t-d) \Leftrightarrow M(\omega)\angle(\theta(\omega)-\omega d)$$

where M(ω) represents magnitude response and
θ(ω) represents phase response

frequency representation given by X(ω). An alternative magnitude and phase representation of this relationship is given on the right side. The Fourier *time scaling* property states that if a signal is scaled in time by a factor α, its frequency spectrum (both Magnitude and Phase) is scaled by a factor 1/α, proportional to frequency, as given by Eq. 3.

$$x(\alpha t) \Leftrightarrow \left|\frac{1}{\alpha}\right| X\left(\frac{\omega}{\alpha}\right) \text{ or } x(\alpha t) \Leftrightarrow \left|\frac{1}{\alpha}\right| M\left(\frac{\omega}{\alpha}\right)\angle\theta\left(\frac{\omega}{\alpha}\right) \qquad \textbf{Eq. 3.}$$

This expression indicates that irrespective of the shape and start time of the signal, any variation (scaling) in the i_{DDT} width can be tracked exactly by its phase spectrum. TSA's delay estimation procedure takes advantage of these properties by computing Phase Signature Waveforms (PSWs) from the Fourier phase spectra of i_{DDT}s. A PSW represents the difference waveform obtained by subtracting the Phase spectrum of the i_{DDT} measured in a test chip from that of a reference chip. Figure 6 shows the PSWs of 13 simulated chips, representing process models *b* through *n*, computed with respect to reference model *a*.

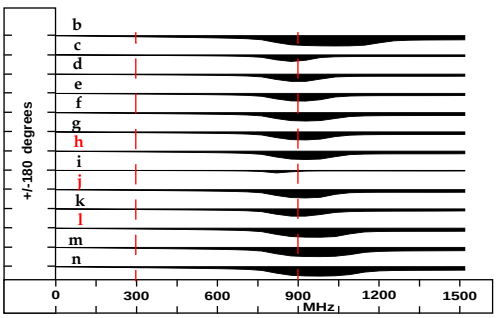

Fig. 6. Phase SWs from 14 process simulations under slow path sensitization.

The area under the PSWs is computed within the desired frequency band (300-900MHz in Figure 6) to obtain a single quantity, referred to as PSWA. Figure 7 shows the cross correlation of PSWAs against the relative slow path delay. The correlation coefficient (CC) of 99.6% indicates that the relationship between the PSWA of i_{DDTsp} and the corresponding path delay is linear.

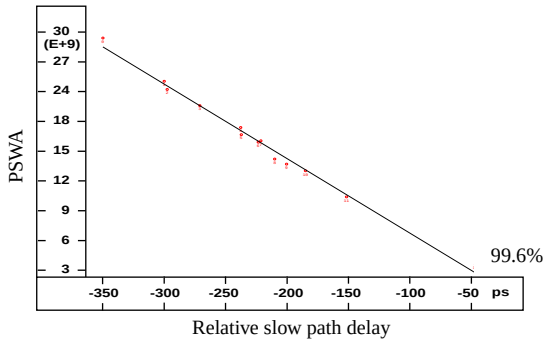

Fig. 7. Phase SWA vs. relative slow path delays.

The linearity of this relationship is based on the property of the Phase spectrum to uniquely track the features in the i_{DDT}s that are most sensitive to delay variations, such as their widths. This result indicates that under the constraint of single path sensitization (or correlated multiple path sensitizations), Fourier analysis of i_{DDT} is capable of tracking a limited number of global events, such as rising and falling edges, in the i_{DDT} waveform. However, the i_{DDT}s generated from chips with multiple, weakly correlated path delays require the tracking of several features, as discussed above in reference to Figure 5. In this case, the accuracy of estimating both path delays using Fourier analysis is degraded since our procedure produces one quantity, a PSWA, where two are needed.

For example, Figure 8 plots the PSWAs of the composite-i_{DDT} against the delay of the fast (top) and slow (bottom) paths under dual path sensitization. The markings on the y axis correspond to the fast path PSWAs; the slow path data points have been shifted down to make it easier to distinguish between the two sets of points. The CC for each analysis are given as 98.8% and 68.2%, respectively. (The quantities inside the parenthesis represent the "ideal" CCs obtained from simulation experiments in which each of the paths are sensitized individually.) The single-path tracking limitation of Fourier analysis is clearly reflected in this analysis, which shows that the PSWAs track the fast path delay more accurately than the slow path delay.

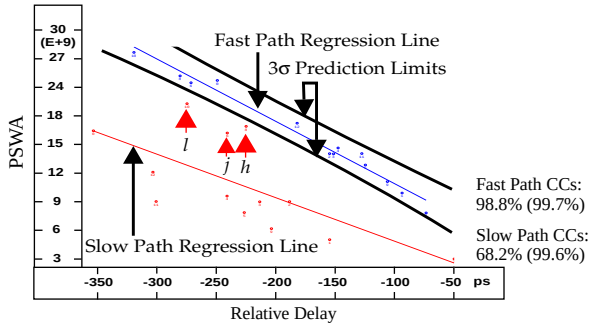

Fig. 8. Phase SWAs vs. fast (top) and slow (bottom) relative path delays.

The higher degree of correlation between the PSWAs and the fast path delay can be attributed to the "weighted average" property of Fourier phase, given by Eq. 4 and Eq. 5. Eq. 4 indicates

$$ACos(\omega t + \Phi) = A_1 Cos(\omega t + \Phi_1) + A_2 Cos(\omega t + \Phi_2) \ldots = \sum_{i=1}^{N} A_i Cos(\omega t + \Phi_i) \quad \textbf{Eq. 4.}$$

that the superposition of cosinusoidal waveforms with the same frequency ω but with different amplitudes A_i and phase-angles Φ_i, generates a cosinusoid of the same frequency ω with amplitude A and phase-angle Φ. Eq. 5 indicates that the resultant phase angle Φ can be approximated as a weighted average of the individual phase angles Φ_i. Since the amplitude of i_{DDTfp} is much higher

$$\Phi \approx \frac{\sum_i A_i \Phi_i}{\sum_i A_i} \quad \textbf{Eq. 5.}$$

than that of i_{DDTsp}, the composite-i_{DDT} phase spectrum is weighed towards the phase spectrum of the fast path, yielding a better estimation of its delay.

In summary, Fourier analysis is capable of providing accurate estimates of path delays for cases in which the path delays remain correlated across regions of the chip (or when it is possible to sensitize one path at a time) [3]. If transistor dimensions vary widely, then the accuracy of estimating multiple path delays is reduced under Fourier analysis because of its inability to track multiple features of a signal simultaneously. Under such conditions, a wavelet transform (WT) can be used to improve prediction accuracy.

6 Path Delay Estimation using Wavelets

Time-frequency analysis, unlike Fourier analysis, partitions the time domain signal into smaller sections using localized window functions. Each section is decomposed into an alternate representation using Fourier basis functions (sine/cosines) or wavelets.

The advantages of time-frequency analysis over Fourier analysis are two fold. First, the ability to analyze frequency components in a specific time interval makes it an effective method for decomposing *non-stationary* signals whose frequency content change over time. However, the frequency content of the gate i_{DS} waveforms vary over a narrow frequency band, which suggests that i_{DDT} waveforms are well characterized as stationary. Therefore this advantage of time-frequency analysis cannot be leveraged for delay estimation purposes in defect-free chips. (It is noted that the frequency content of a defective gate's i_{DS} typically occupies a lower and/or wider frequency band and consequently, this feature of time-frequency analysis may be useful for defect detection purposes). A second advantage of time-frequency analysis is the ability to localize events in time. This means it can provide frequency information localized to corresponding time intervals in a signal. The ability of time-frequency analysis to localize more than one feature in a signal makes it suitable for tracking multiple independent delays in i_{DDT} waveforms. This capability comes at the cost of increased computational complexity, however, as described in Section 7.

Time-frequency analysis based on the wavelet transform (WT) uses wavelet basis functions derived from a mother wavelet. Wavelets are finite in length and have a characteristic shape that dictate the distribution of their frequency content. The frequency and time resolution of wavelets is varied by applying shifting and scaling operations to the mother wavelet. Eq. 6 gives the expres-

$$W(s,\tau) = \int x(t)\Psi_{s,\tau}(t)dt \qquad \textbf{Eq. 6.}$$

$$\Psi_{\tau,s}(t) = \frac{1}{\sqrt{s}}\Psi\left(\frac{t-\tau}{s}\right) \quad s = \text{scale } \tau = \text{shift (or translation)}$$

sion for a continuous wavelet transform (CWT) of a signal x(t). The *s* parameter is the scaling factor and the τ parameter is the translation factor (shift) that are applied to the mother wavelet, $\Psi_{\tau,s}(t)$. The factor $s^{-1/2}$ normalizes energy across the different scales. As *s* changes, the wavelet covers different frequency ranges, with larger values corresponding to small frequencies. The time localization center of the wavelet in the signal is changed through parameter τ.

Proper selection of the mother wavelet plays an important role in the ability of a WT to extract signal features. Wavelets are generally categorized based on their compactness in the time and frequency domain and their smoothness. Wavelets that are characterized by sharp changes (less smooth) are more capable of tracking discontinuities or abrupt changes in a signal, whereas, wavelets with smooth curves are more capable of tracking the global features of the signal.

In this paper, we determine the i_{DDT} feature extraction capabilities of two mother wavelets, Haar and Mexican-Hat, shown in Figure 9. The Haar wavelet, denoted by h(t), is characterized by a sharp change in its shape. In contrast, the Mexican-Hat wavelet, denoted as m(t), is fairly smooth. The Haar wavelet inherently has good time localization, which suggests that it is better at locating sharp changes in a signal, such as the starting and ending transitions of the i_{DDTfp} in the composite-i_{DDT} shown in Figure 5.

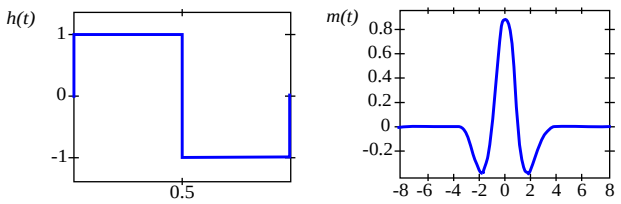

Fig. 9. Haar (left) and Mexican-Hat wavelets (right).

Figure 10(b) shows the CWT of the i_{DDT} waveform shown in Figure 10(a), obtained using the Haar mother wavelet. Figure 10(b) is essentially a 3D-plot, showing the absolute values of the wavelet coefficients as a grayscale gradient, with scales (*s*) plotted along the y-axis and time-shift (τ) along the x-axis. The darker regions in the plot represent coefficients with larger absolute magnitudes. The lower portion of this figure shows the coefficient values at finer scales (high frequencies) for all possible time-shifts. The ability of the Haar CWT to locate sharp changes in the i_{DDT} waveform is exemplified by the inward tapering of the two funnel-shaped dark regions towards the bottom of the plot. These time positions correspond to the starting and ending transitions of the fast path in the composite-i_{DDT} (Figure 10(a)). At higher scales, the dark region starts to broaden, and begins to track the more slowly changing features in the i_{DDT} waveform. Figure 10(c) plots the coefficients for *s* = 64, illustrating that the dark regions in the CWT actual correspond to the both local minima and maxima in the coefficients.

From these observations, it follows that the time interval between the minima and maxima at lower scales, denoted as $t_{max-min}$ in Figure 10(c), should be well correlated with the fast path delay. Bear in mind that very low scale values correspond to fre-

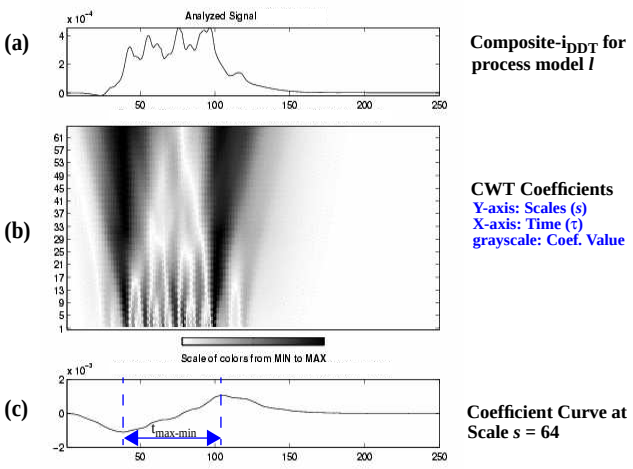

Fig. 10. CWT (b) of process model *l* i_{DDT} waveform (a) using Haar wavelet. (c) gives the wavelet coefficient curve at scale s=64.

quencies that cannot be measured (at any significant amplitude) in the testing environment. For example, *s*=20 corresponds to a frequency band centered at 5GHz. Therefore, any practical application must restrict scales to *s*>=50 (~2GHz). In spite of this restriction, the *s=82* scale yields the highest level of correlation (99.37%) with the fast path delays across the 14 process models. Figure 11 shows the scatterplot of $t_{max-min}$ versus the relative fast path delay. The scale *s*=82 corresponds to a frequency band centered around 1.2GHz, derived using Eq. 7.

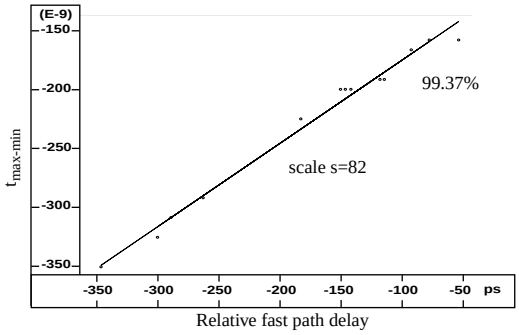

Fig. 11. $t_{max-min}$ vs. relative fast path delays from simulations under simultaneous dual path sensitization.

$$f = \frac{F_c}{\Delta \bullet s} \qquad \textbf{Eq. 7.}$$

where F_c is the center frequency of the wavelet spectrum (Hz)
Δ is the sampling period and *s* is a scale

The Haar wavelet also tracks the slow path delay, but does so at higher scales. The scale *s*=234 (~437MHz) gives the highest CC in this case. Figure 12 shows the scatterplot of $t_{max-min}$ vs. fast path delay at this scale. The computed CC of 95.4% is significantly larger than corresponding value of 68.7% obtained using Fourier analysis.

The CWT analysis of the 14 composite-i_{DDT} waveforms using the Mexican-Hat wavelet yields similar results for the fast path analysis but slightly worse results for the slow path analysis. Figure 13(b) shows the CWT of the process model *l* composite-i_{DDT} waveform. The signal decomposition is noticeably different under the Mexican-Hat and Haar wavelet functions. For example,

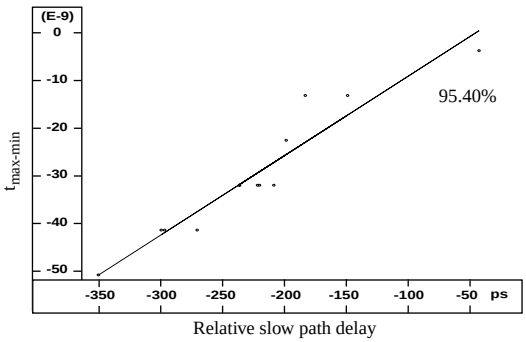

Fig. 12. $t_{max-min}$ vs. relative slow path delays from simulations under simultaneous dual path sensitization.

the coefficient curve shown in Figure 13(c) resembles a segment of a cosinusoid curve. The dark region enclosed between the bright-white lines in Figure 13(b) represents the local maxima of the coefficient curves. For scales lower than *s*~16, the dark region bifurcates into two portions (two maxima) that taper to time locations corresponding to the sharp transitions of the i_{DDT} waveform shown in Figure 13(a). This shows the basic capability of the CWT to track sharp features at lower scales. The occurrence of a single maxima at higher scales reflects its ability to track global features of the signal.

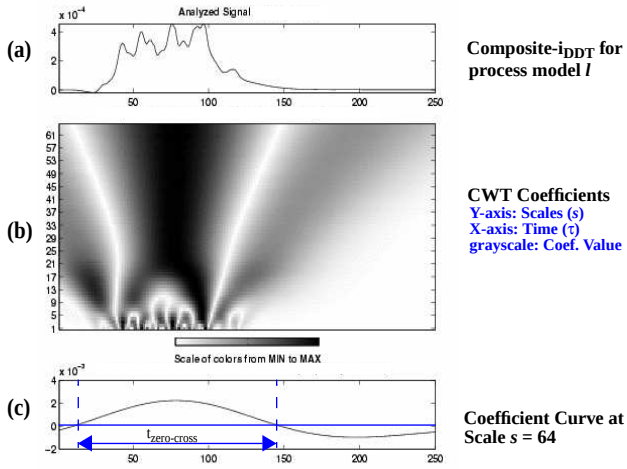

Fig. 13. CWT (b) of process model *I* i_{DDT} waveform (a) using Mexican-Hat wavelet. (c) gives the wavelet coefficient curve at scale s=64.

The time interval $t_{zero-cross}$ shown in Figure 13(c) delimits the time interval between the points defined when the coefficient curve becomes zero. The scales that yield the highest CCs in the corresponding $t_{zero-cross}$ vs. fast path and $t_{zero-cross}$ vs. slow path delay plots (not shown) are *s*=22 (CC=99.3%) and *s*=61 (CC=90.0%), respectively. For the Mexican-Hat CWT, these scales correspond to a frequency band centered around 1.16GHz and 420MHz respectively.

7 Complexity Analysis

An analysis of the computational complexity of the DFT and CWT-based procedures completes their comparison. The computation of X(ω) defined by Eq. 1 for a given ω requires 2N multiplications and 2N additions. There are N/2 frequencies in the complete spectrum yielding a complexity of $O(N^2)$. However, our DFT-based delay estimation procedure analyzes only a constant band of C frequencies (with C in the range of 5-10) and therefore the complexity reduces to O(N).

The computation of the CWT defined by Eq. 8 entails N^2 multiplications and N^2 additions, yielding a complexity of $O(N^2)$. Note that a continuous wavelet transform is required (as opposed to a discrete wavelet transform (DWT)) because all time positions must be analyzed in order to adequately localize time events. Alternative, more efficient algorithms for computing the DWT are not useful because our analysis shows that the best delay estimation is obtained at scales that are not dyadic. Moreover, the delay estimation accuracy is sensitive to the incremental shift in the wavelet (τ). Therefore, the complexity of wavelet transform for this procedure cannot be further reduced using efficient filtering algorithms applicable to DWT.

$$C(\tau, s) = \sum_{n=0}^{N-1} x(n)\Psi\left(\frac{t-\tau}{s}\right) \qquad \textbf{Eq. 8.}$$

Where s denotes a scale value [s=1,2.....N-1]
n denotes a discrete time sample [n=0,1,2.....N-1] and
t denotes a incremental time shift [t=0,1,2.....N-1]

8 Conclusions

This paper compares the prediction accuracy and complexity of Fourier and wavelet analysis techniques for path delay estimation. Wavelet analysis of i_{DDT} is more accurate than Fourier analysis for predicting multiple delays in custom circuits that incorporate paths constructed with transistors of widely varying widths. The cost of increased accuracy is increased computational complexity, $O(N^2)$ vs. O(N), respectively. Two wavelets, Haar and Mexican-Hat are investigated. Both wavelets track the fast path delays more accurately using lower scales (corresponding to ~1GHz), while higher scales (~400MHz) more accurately track slower path delays. The Haar performs slightly better than the Mexican-Hat for slow path delay predictions.

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