An Automated Technique to Identify Defective CMOS Devices based on Linear Regression Analysis of Transient Signal Data

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Abstract

Transient Signal Analysis is a digital device testing method that is based on the analysis of voltage transients at multiple test points and on I_{DD} switching transients on the supply rails. We show that it is possible to identify defective devices by analyzing the transient signals measured at test points on paths not sensitized from the defect site. The small signal variations generated at these test points are analyzed in both the time and frequency domain. Linear regression analysis is used to show the absence of correlation in these signals across the outputs of bridging and open drain defective devices. A statistical method and an algorithm for identifying defective devices are presented that is based on the standard deviation of regression residuals computed over a compressed representation of these signals.

1.0 Introduction

Transient Signal Analysis (TSA) [1] is a parametric approach to testing digital integrated circuits. Defect detection is accomplished in TSA by analyzing the transient signals of a device measured simultaneously at multiple test points. The approach offers two distinct advantages over other logic and parametric testing methods. First, device coupling mechanisms permit the detection of defects at test points that are not on logic signal propagation paths from the defect site (off-path nodes). Consequently, direct observation of logic faults is not necessary in TSA. Second, the cross-correlation of multiple test point signals allows signal variations caused by process tolerances to be distinguished from those caused by defects. This is true because process tolerance effects tend to be global, causing signal changes on all test points of the device. In contrast, signal variations caused by a defect tend to be regional and more pronounced on test points closest to the defect site [2].

In this paper, we focus on the development of a statistical method that can be used to automate the TSA testing process. We introduce Signature Waveforms (SWs) as a means of capturing signal variations between defect-free and defective devices and formulate a statistics based on a compact representation of the SWs called Trapezoidal Rule Areas (TRAs). We evaluate the effectiveness of the TRAs in capturing the signal variations observable in the SWs separately in the time and frequency domain. The evaluation is performed by analyzing the TRAs from test point pairing of defect-free and defective devices using linear regression. The regression line computed for each pairing of the TRAs of defect-free devices tracks the variations introduced by process tolerances. The deviations or residuals of the TRAs of defective devices are computed with respect to the regression lines and are summarized in a statistic, the standard deviation. The standard deviations computed for defect-free and defective devices are compared to determine the effectiveness of the TRAs in capturing the signal variations introduced by defects.

The analysis is performed using the time, Fourier magnitude and phase SWs obtained from four hardware experiments. One experiment is used as a control experiment to evaluate error in the estimates of the regression lines. The results of the three remaining experiments show that the phase TRAs are consistent with the signal behavior observed in the SWs and are best able to capture the variations produced by defects. Based on these results, we propose an algorithm that can be used to automate the detection of defects.

2.0 Background

Parametric device testing strategies [3] are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of quiescent supply current or transient response. Many types of parametric tests have been proposed [4] but recent research interest has focused primarily on three types; I_{DDQ} [5], I_{DD} [6], and delay fault testing [7].

I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value. I_{DDQ} has been shown to be an effective diagnostic technique for CMOS bridging defects, but is not applicable to all types of CMOS defects [8]. Recently, concerns have been raised over the applicability of IDDQ to deep

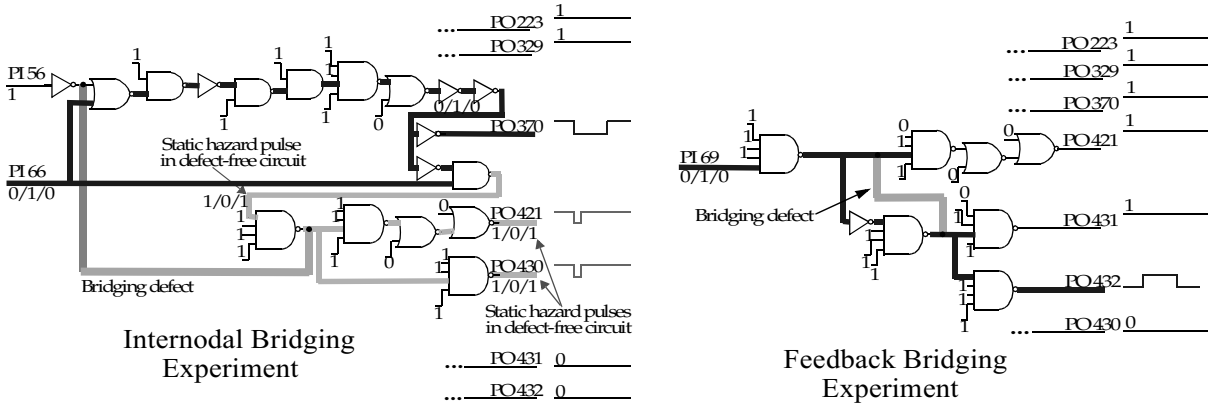

Figure 1. Portions of the c432 showing the sensitized paths from the Bridging Experiments.

sub-micron technologies [9].

Several dynamic supply current I_{DD}-based approaches have since been proposed to overcome the limitations caused by the static nature of the I_{DDQ} test [10][11][12]. In general, these I_{DD}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however, however, they do not provide a means of accounting for process tolerances and are therefore subject to aliasing problems. Alternatively, delay fault testing takes advantage of the fact that many CMOS defects cause a change in the propagation delay of signals along sensitized paths. Difficulties with delay fault testing include the complexity of test generation and path selection [13]. Franco and McCluskey [14] and others [15][16] have proposed extensions to delay fault testing that address some of these difficulties.

3.0 Experiment Summary

In this section, we present a summary of the experiment setup and show the types and locations of the defects that we introduced into a set of test devices. We conducted hardware experiments on three versions of the ISCAS85 c432 benchmark circuit: a version with intentionally inserted bridging defects, a version with intentionally inserted open drain defects and a defect-free version. Four devices of each version were fabricated. The four defect-free devices and one set of either the open drain or bridging defective devices were used in each experiment. Four experiments were conducted, two bridging experiments labeled Internodal-Bridging and Feedback-Bridging, and two open drain experiments labeled Open-Drain and Control.

The signal measurements were taken on core logic test test pads placed on the output nodes of the gates driving the seven primary outputs, labeled 223, 329 370, 421, 430, 431, and 432. I_{DD} was also measured on V_{DD} as an eighth output signal.

Figure 1 shows portions of the schematic diagram from the c432 for the bridging experiments. The dotted line in the figure represents the bridging defect which was created in the layout by inserting a first-level to second-level metal contact between the output lines of a 4-input NAND gate and an inverter. In the defect-free devices, a static hazard causes a pulse to propagate to POs 421 and 430 along paths shown shaded in the figure. Since the output of the inverter driven by PI 56 is low, the bridge eliminates the pulse in the bridging defective devices. The left side of Figure 1 shows the sensitized paths for the Feedback Bridging experiment. Although the defect is on a sensitized path driving PO 432, the circuit operates logically correctly under this test sequence. The bridging defect is shown in the figure as a dotted line but is physically represented as an extra piece of second-level metal between the outputs of two 4-input NAND gates.

Figure 2 shows the sensitized paths through the defective gates for the Open Drain (top) and Control experiments (bottom). The left side of Figure 2 shows an open drain defect in the transistor-level schematic diagram of a 4-input NAND gate. A three micron wide piece of first-level metal has been removed between the p-transistor drain pairs. Both of the open drain experiments test this type of defect in two different NAND gates in the circuit. The test sequence for the Open-Drain experiment generates a number of pulses which are created by a static hazard in the defect-free devices but eliminated by the defect in the open drain devices.

The Control experiment was designed to test the change in loading capacitance introduced by the defect on POs 329 and 370. However, the test sequence for the Control experiment does not produce measurable changes in parametric behavior of the Open-Drain devices. Since the Open-Drain devices behave like defect-free devices under these conditions, we use this experiment as a control experiment to evaluate the error in the regression line estimates. We later show that these same Open-Drain devices can be identified as defective when tested using an input stimulus that causes a fault (Open-Drain experiment). Moreover, since the

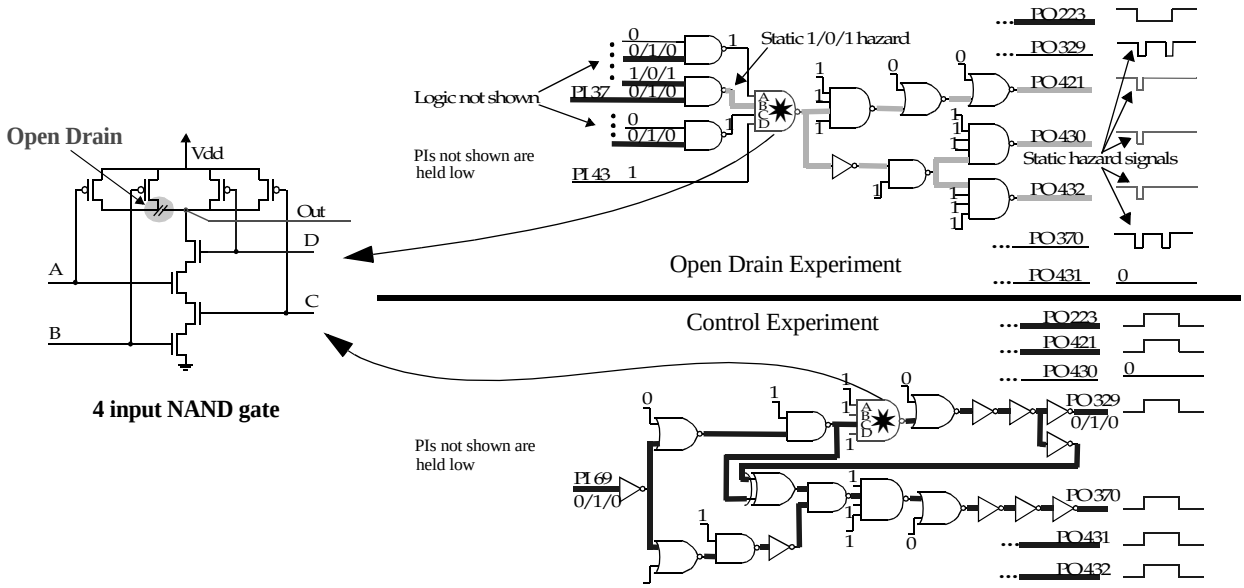

Figure 2. Portions of the c432 showing the sensitized paths from the Open Drain and Control Experiments.

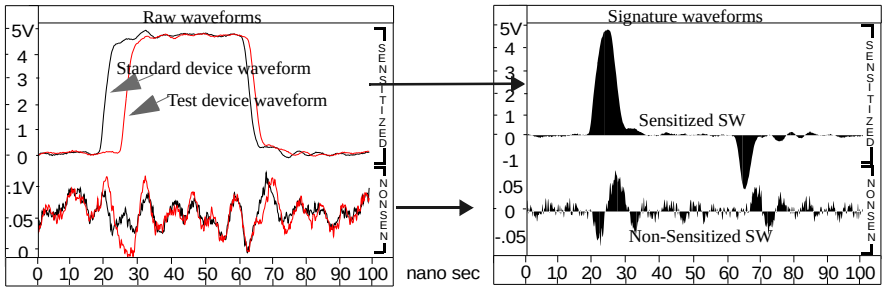

Figure 3. Time Domain Signature Waveforms.

emphasis of these experiments is on the measuring the coupled variations introduced by the parametric faults at the test points, we analyze only the transient signals of test points that are not directly affected by parametric or logic faults.

4.0 Testing Method

We use **Signature Waveforms** or **SWs** to capture signals variations between devices as shown in Figure 3. The plot labeled “Raw Waveforms” depicts the transient waveforms of two devices. The waveforms shown along the top of the plot were measured on test points that were driven by a sensitized path. The waveforms shown along the bottom were measured on non-sensitized test points. We create Time Domain Signature Waveforms from these pairs of transient waveforms by subtracting the test device waveform from the standard device waveform. The difference waveforms, shown in the right plot of Figure 3, are shaded along a zero baseline in order to emphasize the signal variations. We also analyze the frequency domain representation of the transient signals by creating frequency domain Signature Waveforms. The magnitude and phase components produced by a Discrete Fourier Transform of the raw time domain waveforms are used to generate Magnitude and Phase SWs by subtracting the test device magnitude and phase values from the corresponding values of the standard device. In order to simplify waveform post-processing, we compress the multi-point SWs into a single floating point value by computing the area under their curves using a Trapezoidal Rule integration method. We call the area value result a TRA.

Figure 4 shows the Fourier Phase SWs from two non-sensitized test points, 329 and 432, of an hardware experiment involving one standard and seven test devices. The top-most waveform is the output trace of a defect-free device that is used as the standard. The SWs of three additional defect-free devices are labeled DF#*x* while the SWs of four BRidging defective devices are labeled BR#*x*. The TRAs shown to the right of each plot are computed over the portion of the frequency range between 10 to 250 MHz

The statistics that we use to detect defects are based on standardized residuals. Standardized residuals are derived from two dimensional scatter plots of TRAs. For example, the TRAs shown in Figure 4 define a scatter plot of 7 data

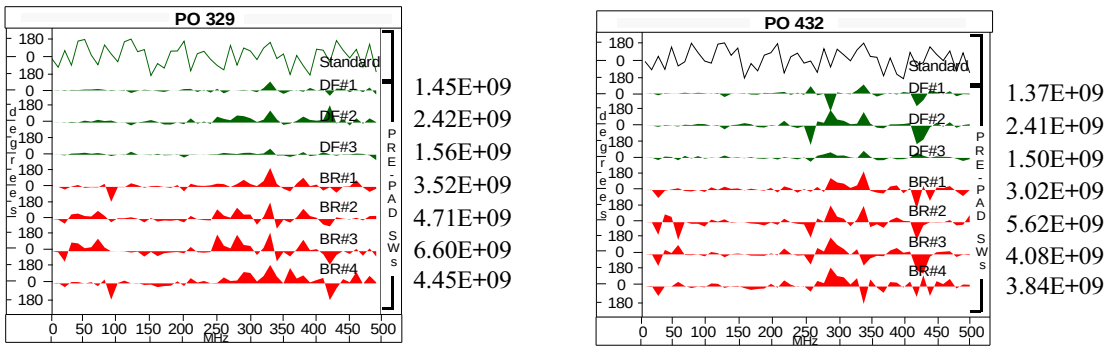

Figure 4. Example Fourier Phase SWs and TRAs from test points 329 and 432.

σ	Experiment			
Device/Experiment	**Control**	**Open-Drain**	**Internodal-Bridge**	**Feedback-Bridge**
OD/BR#1	3.57	**425.62**	214.58	48.21
OD/BR#2	**4.21**	434.79	227.15	91.82
OD/BR#3	1.63	556.87	**117.59**	120.26
OD/BR#4	3.01	514.93	303.64	**40.81**
DF_{Max}	0.18	0.80	0.76	0.68

Table 1: Summary of Phase σ Statistics.

points in which the x values are defined by PO 329 and the y values by PO 432. Scatter plots of other combinations of the test points are defined in a similar way. We compute a least squares estimate of the regression line through the three defect-free data points of each scatter plot. Data point residuals are computed as the distance along the y axis between the data points and the regression line and are standardized by dividing by the mean square error of the 3 defect-free data points.

In [1][2], we show that a high degree of linear correlation exists among the data points of defect-free devices in these scatter plots. This is consistent with our observations that variations in SWs resulting from process tolerance effects occur in all test point signals. Therefore, the regression line tracks process tolerance effects and, in the absence of unmodeled random variables such as measurement noise and intra-device process tolerances, the data points of defect-free devices would be co-linear. Instead, the data points of defect-free devices are distributed around the regression line and define a region that we call the process tolerance zone. It is in this region that we expect to find the data points of defect-free devices.

In contrast, we have observed that defects introduce additional variation in the SWs of defective devices that varies depending on the state and position of the test point with respect to the defect site. This causes the data points of defective devices to fall outside of the process tolerance zone. Therefore, the standardized residuals of defective devices capture uncorrelated variation that results from defects in addition to the variation common to all data points, namely, that due to measurement noise, intra-device process tolerances and error in the regression line estimate

Our defect detection criteria is based on the standard deviation, σ, of the set of standardized residuals obtained for each device over all possible pairing of the test point signals. For example, if the transient signals from six test points are used in the analysis, then fifteen scatter plots are derived. In our experiments, each scatter plot contains 7 data points, 3 from defect-free devices and 4 from defective devices. The standard deviation of the fifteen standardized residuals belonging to each device are computed with respect to their regression lines. σ measures the dispersion of the data points around the regression lines.

5.0 Regression Analysis

Due to space limitations, we show only the Fourier phase σ statistics, which are superior to both the time and Fourier magnitude results. Table 1 shows the standard deviations computed in the four hardware experiments. The left-most column identifies the device with, OD indicating Open-Drain and BR indicating BRidging. The σ statistic of each of the four experiments are shown in columns two through five. The shaded value in column two is the maximum among the defective device values while the shaded values in columns three, four and five are the minimum values. The bottom row depicts the maximum Defect-Free σ statistic for each experiment.

Several characteristics are notable in these results. First, the smallest minimum σ statistic, given in column five as 40.81, is nearly a factor of ten larger than the regression line error estimate of 4.21 given in column two. Therefore, the σ statistic is able to capture the signal variation caused by the defect to a significant degree. Second, there is consistency between the magnitude of these values and the amount of variation introduced by the defect. For example, we can rank each of the experiments by counting the number of sensitized paths disrupted by the defect. The test sequence used in the Open-Drain experiment causes faults on three sensitized paths. The test sequence of the Internodal-Bridging experiment causes faults on two sensitized paths while the test sequence used in the Feedback-Bridging experiment causes a fault on a single sensitized path. Except of a single instance, the rank of the σ statistics correspond to this ordering as shown from left to right along each row of columns three through five. This correspondence is not unexpected since each of the faulted paths contribute to off-path signal variation.

The σ statistics provide the basis on which a defect detection algorithm can be devised. We recognize that any type of device testing method requires a test vector generation strategy and we are currently investigating this issue. Given a set of suitable test vector pairs and a set of known defect-free devices, device testing can be carried out as follows. The regression lines of pairing between selected test point signals are derived and the σ statistics computed under each of the test sequences. A second set of known defect-free devices are used to evaluate the error in the regression line estimates and the process is repeated until the error is acceptably small. The process tolerance zones based on 1 - α confidence limits are derived under each test sequence. The σ statistic of each test device is then computed and compared against the process tolerance zone limits. If a σ statistic falls outside of the process tolerance zone under any of the test sequences, the device is marked as defective.

6.0 Conclusions

We presented a statistical technique to identify defects in digital integrated circuits that is based on linear regression analysis of transient signal data. Since the number of test devices in our experiments was small, we estimated the error in the regression lines using a control experiment and found the regression lines to be reasonably estimated. We compared the σ statistics of this experiment with those obtained from three defective device experiments and determined that the Fourier phase analysis yielded values that were consistently larger than the time domain and Fourier magnitude analysis with respect to the regression line estimation error. Therefore, the Fourier phase TRAs provide the highest degree of confidence that a positive defect detection decision is correct. Based on these results, we proposed an algorithm to automate the detection of defects in TSA.

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