Hardware Results Demonstrating Defect Localization Using Power Supply Signal Measurements

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Abstract

The power supply transient/quiescent signal (I_{DDT}/I_{DDQ}) methods that we propose for defect localization analyze regional signal variations introduced by defects at a set of power supply ports on the chip under test (CUT). The methods are based on the comparison of the CUT with a golden reference chip, either simulated or determined to be defect-free, with the objective of distinguishing anomalous signal behavior introduced by a defect from that introduced by process variations. However, variations in contact resistance between the probe card and the CUT introduces anomalies in the measured power supply signals that complicates the task of comparing data between chips. This paper presents hardware results that demonstrate the effectiveness of a previously developed calibration technique designed to eliminate these types of signal anomalies introduced by the testing environment. The CUT hardware data presented in this work is calibrated using simulations of the CUT's power grid and special on-chip sources of stimuli called 'calibration circuits'. Several novel Look-Up Table based defect localization techniques are proposed that analyze the calibrated power supplies signals. The results of predicting the locations of emulated defects in nine copies of a test chip demonstrate the effectiveness of the techniques.

1.0 Introduction

The Test and Test Equipment section of the 2003 edition of the International Technology Roadmap for Semiconductors (ITRS) indicates that traditional Physical Failure Analysis (PFA) is facing significant challenges [1]. The objective of PFA is to determine the root cause of failure in an IC**.** The major steps in PFA include fault localization, deprocessing and physical characterization of the defect. However, as CMOS technology migrates to smaller feature sizes, more complex devices and additional metallization layers, PFA is becoming slower and more difficult to be performed routinely. ITRS indicates that the role of PFA is likely to shift to a "verification" process as software-based localization methods continue to improve.

The localization method proposed in this work can be classified as "a non-destructive software-based method" because it is based on the analysis of electrical signals measured under normal testing conditions. Unlike other logic based fault localization techniques, the method proposed here analyzes power supply currents (I_{DDT}/I_{DDQ}). Unfortunately, any method based on the analysis of analog signals is challenged by the "analog baggage" that naturally accompanies such techniques. For example, I_{DDT} (and I_{DDQ}) methods require a well defined threshold between good and bad chips that does not erroneously degrade yield or quality. Factors that contribute to the difficulty of defining this threshold include process variations and variations in the testing environment itself.

Since our proposed method for defect localization analyzes power supply currents through multiple supply pads on the chip, the impact of variations due to the testing environment are more pronounced than they are for traditional approaches such as techniques that analyze a single global I_{DDQ} or I_{DDT} measurement [9][11]. More specifically, variations in probe card contact resistance have a significant impact on the distribution of currents through each of the supply ports, which adversely affects the resolution of our defect localization method. In previous work, we developed a calibration method to eliminate probe card variations (and performance variations) using simulation experiments [4]. The hardware chips analyzed in this work verify the effectiveness of the calibration method described in [4].

Once the variations due to the testing environment are calibrated for, it then becomes possible to develop reliable detection and localization methods using the multiple supply pad signal measurements. In this work, we develop Look-Up based defect localization techniques that exploit multiple supply pad measurements. Experiments conducted on nine hardware chips show that it is possible to predict the location of emulated defects with reasonable accuracy in the presence of extreme probe card contact resistance variations.

2.0 Background

Advances in silicon technology has imposed challenges on failure analysis (FA) [5]. With every generation, transistor feature sizes, interconnect dimensions and supply voltages are decreasing. On the other hand chip performance, transistor density and number of interconnect layers are on the rise. These trends in addition to advancements in packaging technology like flip-chip bonding has made FA a daunting task. As the 2003 edition of the ITRS indicates,

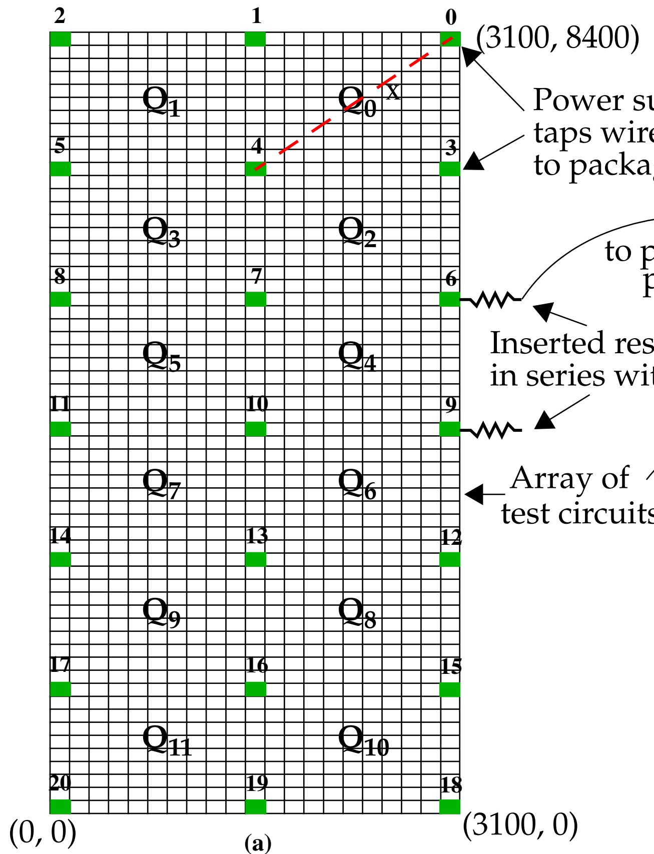

Figure 1. Test CUT.

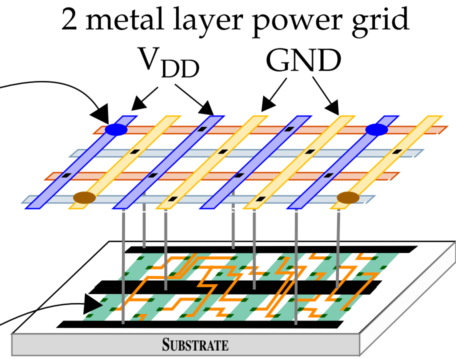

Figure 2. Test CUT's power grid.

the main challenges in FA in the near future are mostly in failsite isolation in dense flip chip parts and high performance parts.

There are two general approaches for failsite isolation. The first category consists of software based techniques and the second category consists of hardware based techniques which exploit secondary effects like heat and light to isolate defects. Hardware based techniques require equipment such as Scanning Electron Microscopes and a variety of specialized detectors. Software based techniques on the other hand are comparatively inexpensive. These techniques use data gathered from the tester in conjunction with simulation results to isolate defective regions of a failed chip. Techniques such as cause-effect [6][7] and effect-cause [8] are routinely used in the industry for fault localization. Some of these techniques require fault dictionaries which store the behavior of a fault for every vector in the test set. Researchers have also investigated using current (I_{DDQ}/I_{DDT}) testing methods either stand alone or in conjunction with logical test data for fault localization [3][4][9]-[19].

3.0 CUT Characteristics

3.1 CUT Design

A block diagram of the CUT investigated in this work is shown in Figure 1. It consists of a 60 by 21 two-dimensional array of test circuits. Each test circuit can be individually excited to provide a test stimulus to the power grid, by itself or in combinations with other test circuits in the array. The power grid is wired in two metal layers as shown in Figure 2. A set of 21 power supply taps, labeled 0 to 20 in Figure 1, emulate the multiple connection points of a typical power grid used in commercial designs. These taps will subsequently be referred to as V_{DDx} where *x* represents one of the tap connections. In order to emulate probe card contact resistance (R_p), on-chip resistances ranging from 1 Ω to 100 Ω were inserted in series between the tap points and each of the power supply C4 pads as shown on the right side of Figure 1. The entire chip is partitioned into "Quads" which are identified as regions surrounded by 4 V_{DDx} tap points, labeled Q_0 through Q_{11} in Figure 1. Each Quad has a total of 121 test circuits (with the exception of Q_{10} and Q_{11} which have one less row.)

3.2 Calibration Circuits

Our multiple supply port testing methodology is very sensitive to probe card contact resistance variations. Figure 3 shows the physical model of a membrane probe card identifying the source of the contact resistance between the probe card and the C4 solder ball of the CUT. This contact resistance will not only vary from touch down to touch down but also from one supply pad to another. The contact resistance variations will manifest as anomalies in the measured distribution of the multiple supply pad currents. The presence of defects will also cause regional signal anomalies. Therefore, it is difficult to distinguish between testing environment variation and defects using only the currents measured under the logic tests.

To overcome this drawback, we introduced a DFT

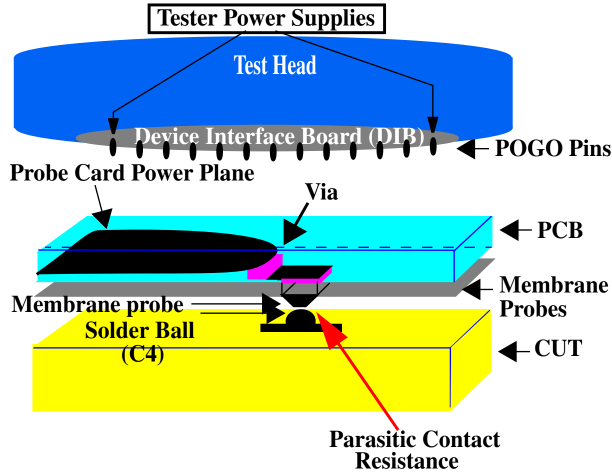

Figure 3. Physical Model of a probe card.

structure called a 'Calibration Circuit' which is described in detail in reference [4]. The basic function of the calibration circuit is to provide stimulus at known locations in the chip. Each CUT calibration cell is excited individually and the corresponding branch current measurements are made at all the supply ports. To compensate for performance variations in the calibration circuit themselves, each of the branch currents are normalized by dividing them by the total current drawn by the CUT. This data is then used in conjunction with the calibration circuit data generated from simulations to calibrate the CUT's branch currents obtained under the logic tests. The details of the procedure will be discussed in a later section. The test circuits at positions shown by the shaded blocks (the V_{DD} tap points) in Figure 1 are designated as the calibration circuits in this work.

3.3 Simulation Models

In order to implement the calibration procedure, we constructed a two layer grid that closely approximates the structure of the actual power grid of the CUT. We derived a resistive model of this power grid using an extraction script that preserved the physical structure of the metal interconnect in the topology of the R network, i.e. no network reduction heuristics were applied[1]. The resistance parameters of the metal layers and vias were chosen as the nominal values for the technology.

1.Bypass capacitance and inductance are also important elements to model in the power grid. Although we expect that it will be necessary to include these elements when this technique is applied to commercial designs, in this work, the simpler resistance-only model provided an adequate representation.

As indicated, the calibration procedure applied in these experiments uses simulation data as a means of defining the current distribution profile of the chip under a specific test environment. Although it is possible to calibrate using a simulation model in which each supply port incorporates a unique probe resistance, a uniform probe resistance model offers an additional advantage. If probe resistance for all supply ports are equal, then the distribution of currents to each of the supply ports is determined solely by the resistance profile of the power grid. This simplifies the task of identifying the source of the current in the chip layout. However, the value of the "uniform" probe resistance used in the simulations impacts the results obtained in the localization method.

In order to study the impact of probe resistance, five simulation models were constructed. Four of the five models used a uniform R_p value for all 21 V_{DD} connections. The R_p values chosen for each of the four models were 1 Ω, 1 mΩ, 8.77 Ω and 30 Ω. These models will henceforth be referred to as S1, S2, S3 and S4 respectively. The 8.77 Ω model was chosen because the parallel combination of 21 8.77 Ω resistors yields the same equivalent resistance as that obtained by the parallel combination of the inserted probe resistances on the CUT. Similarly, the 30 Ω model was chosen because it represents the mean of all the probe resistances on the CUT. The fifth simulation model was constructed to reflect the actual "non-uniform" probe resistances present in the CUT. This model will henceforth be referred to as S5.

A set of 1260 simulations were run on each of these simulation models by placing current sources at each of the (x,y) locations corresponding to the positions of the test circuits on the CUT shown in Figure 1. Twenty one of these locations represent the positions of the calibration circuits. For every location, the branch currents were measured at the 21 supply ports and normalized by dividing by 1mA, the value used for the current source in the simulations. The sequence of all 21 normalized supply port currents (I_{Vdd0} $I_{Vdd1}...I_{Vdd20}$) for a given (x,y) location represents an ordered list and is referred to as **Current Profile Vector** (CPV) for that location. Equation 1 shows the definition of

$$CPV_{x,y} = \left[I_{Vdd0}\ I_{Vdd1}\ \ldots I_{Vdd20}\right]_{x,y} \quad \text{(Eq. 1)}$$

a CPV. The CPV for every location was stored in a database for use in the calibration and Look-Up Table based localization procedure described below.

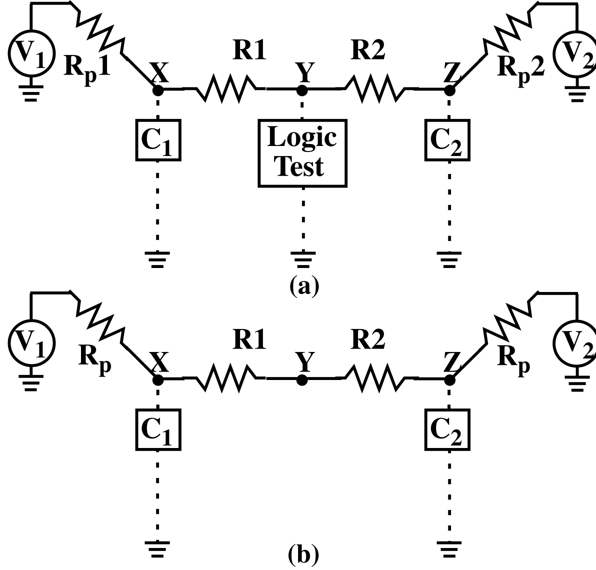

Figure 4. 2-port model (a)Test Case (b)Simulation Case.

3.4 Calibration Procedure

As mentioned in section 3.2, the contact resistances of the probe card will vary not only from touch-down to touch-down but also from pad to pad. The probe card contact resistance variation will distort the natural current distribution determined by the power grid alone. In order to reduce (ideally eliminate) the impact of probe resistance on the current distribution profile, it is necessary to calibrate the measured currents. In this section, we illustrate the basic principles of the calibration procedure using the simple two-port network shown in Figure 4.

The circuit in Figure 4(a) represents the test case and the circuit in Figure 4(b) represents the simulation case. The test case has probe resistances R_{p1} and R_{p2} while the simulation case has a uniform probe resistance of R_p. First the calibration circuit (C_1) at location X is turned on in the test case. The currents through V_1 (I_{1CXT}) and V_2 (I_{2CXT}) are measured[1]. Similarly, currents I_{1CZT} through V_1 and I_{2CZT} through V_2 are measured by turning on calibration circuit C_2. The same procedure is performed on the simulation model generating currents I_{1CXS}, I_{2CXS}, I_{1CZS} and I_{2CZS}. I_{1T} and I_{2T} represent the currents through V_1 and V_2 respectively when a defect at location Y is provoked under a logic test in the test case. Using the eight calibration circuit measurements, the currents I_{1T} and I_{2T} can be transformed into currents I_{1S} and I_{2S} that would have been measured if the test case had uniform probe resistances of R_p. The expressions that relate the test case and the simulation model are shown below in Equation 2.

$$
\begin{aligned}
I_{1CXS} &= a_1 \cdot I_{1CXT} + a_2 \cdot I_{2CXT} \\
I_{2CXS} &= b_1 \cdot I_{1CXT} + b_2 \cdot I_{2CXT} \\
I_{1CZS} &= a_1 \cdot I_{1CZT} + a_2 \cdot I_{2CZT} \\
I_{2CZS} &= b_1 \cdot I_{1CZT} + b_2 \cdot I_{2CZT}
\end{aligned}
\qquad \text{(Eq. 2)}
$$

In Equation 2, a_1, a_2 and b_1, b_2 are constants that redistribute the currents measured through the multiple supply pads. A more convenient representation of the above 4 equations is a matrix form as shown in Equation 3

$$
\underset{A}{\begin{bmatrix} I_{1CXT} & I_{2CXT} \\ I_{1CZT} & I_{2CZT} \end{bmatrix}} \cdot \underset{X}{\begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix}} = \underset{B}{\begin{bmatrix} I_{1CXS} & I_{2CXS} \\ I_{1CZS} & I_{2CZS} \end{bmatrix}} \qquad \text{(Eq. 3)}
$$

In Equation 3, matrix A contains calibration data from the test case, matrix B contains calibration data from the simulation case. This system of equations is solved to obtain the transformation matrix X by computing the inverse of A and multiplying by matrix B. Once the transformation matrix is computed, the test measurements made under a logic test are calibrated using X as shown in Equation 4. Though the expressions shown here are for a 2-V_{DD} port model, the technique can be applied to any n-V_{DD} port model.

$$
\begin{bmatrix} I_{1T} & I_{2T} \end{bmatrix} \cdot \begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix} = \begin{bmatrix} I_{1S} \\ I_{2S} \end{bmatrix} \qquad \text{(Eq. 4)}
$$

In the absence of grid variations and grid modelling inaccuracies, the transformation is exact. To demonstrate this, we applied the calibration procedure to the data obtained from the S1 and S5 simulation models. Recall that S1 had uniform 1 Ω R_ps and S5 had a highly skewed R_p distribution that is representative of the actual CUT resistances. In this case, simulation data from the S1 model was used to calibrate the data from the S5 model.

Figure 5 shows three CPV curves, an **Uncalibrated S5-CPV**, an **S1-CPV** and a **Calibrated S5-CPV**, computed from simulation data obtained when the test circuit at location (2325,7396) (indicated by 'X' in Figure 1) was activated. The y-axis in Figure 5 shows the fraction of the total current drawn from each of the 21 supply ports identified on the x-axis. The **S1-CPV** and **Calibrated S5-CPV** curves are identical, confirming the claim that the transformation is exact. These curves also illustrate the usefulness of the transformation. For example, the large value for V_{DD15} in the **Uncalibrated S5-CPV** curve incorrectly sug-

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1.*A note about the subscripts in I_{pqrs}: p= 1 or 2: voltage source identifier, q='C' denotes that it is a calibration test, r=X,Y,Z: location identifier and s= T,S: test case or simulation case identifier.

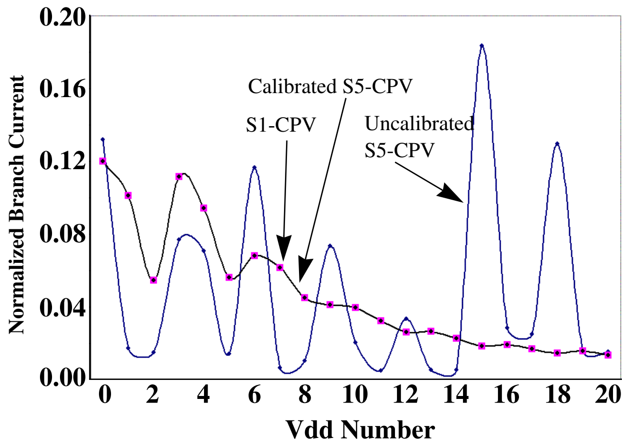


Figure 5. CPVs for location (x,y) =(2325, 7396).

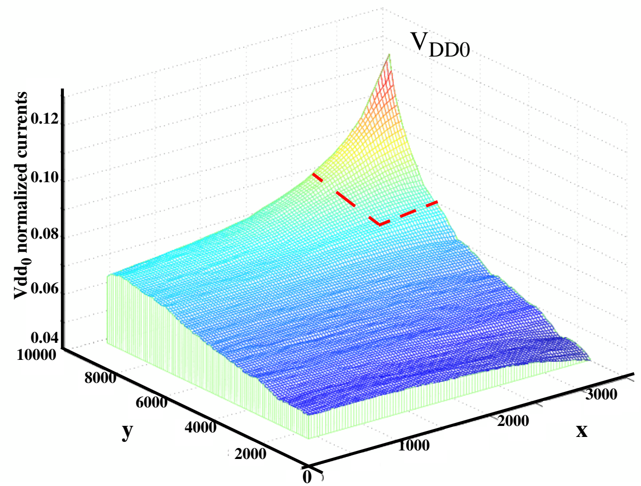


Figure 6. V_{DD0} current profile.

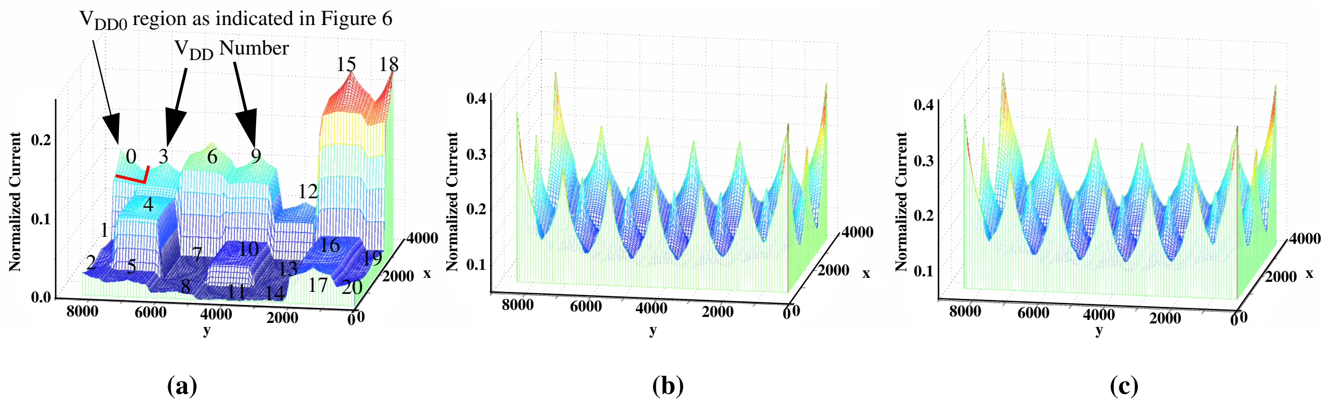


Figure 7. Current profile for (a) uncalibrated hardware (b) simulation (c) calibrated hardware.

gests that the current source is in the vicinity of V_{DD15}. In contrast, the **Calibrated S5-CPV** portrays the expected current distribution in which the largest current is through V_{DD0}, the V_{DD} closest to the source at location (2325,7396).

3.5 Hardware Experiments

The total current and branch currents were measured using Keithley 2400 sourcemeters on a set of 9 chips as each of the test circuits on each chip was individually activated. The branch currents were measured using a custom board that allowed automated switching across the 21 V_{DD} ports. The total leakage and branch leakage currents were also measured in each chip. In this case, no test circuits were enabled. The leakage currents were subtracted from the currents measured with the test circuits enabled.

Figure 6 shows the normalized hardware current profile for V_{DD0} as each test circuit in one of the CUTs was enabled. The x and y axis in Figure 6 represent the location of the enabled test circuit and the z-axis represents the normalized current drawn from V_{DD0}. It is evident from this plot that test circuits in the vicinity of V_{DD0} draw a higher fraction of current from V_{DD0} than test sites that are situated farther away.

The impact of the non-uniform R_ps is best illustrated by constructing a plot in which the currents drawn by circuits in the vicinity of each supply port are *pasted* together, as shown in Figure 7(a). The numbers in Figure 7(a) indicate the supply port from which the current measurements were made, the x and y coordinates represent the spatial locations of the enabled test circuits and the z-axis represents the normalized currents. As an example, the region enclosed with the dotted line in Figure 6 is labeled in Figure 7(a).

From Figure 7(a), it is clear that the fraction of total current drawn by each of the supply ports varies widely and is dependent on the value of R_p. For example the peak values range from 0.87% (for V_{DD7}) to approximately 24.04% (for V_{DD18}). The wide variations are due to the non-uniform R_ps ranging from 1 Ω to about 100 Ω. This scenario is quite exaggerated as compared to the real testing environment. Probe card contact resistances are usually in the vicinity of 250 mΩ [20]-[22]. Therefore, this test setup represents a worst case scenario.

The uncalibrated hardware measurements shown in Figure 7(a) are difficult to use for any type of defect localization procedure because the overwhelming effect of the non-uniform R_ps overshadow the regional behavior of the power grid. It is therefore necessary to calibrate this set of current measurements using a reference model with known R_ps.

Figure 7(b) shows the normalized currents measured at each of the supply ports obtained from the S1 simulation model, displayed using the same format as that described for Figure 7(a). Here it can be seen that the uniform R_p model causes the currents to distribute in a fairly uniform manner to each of the supply ports. The peak values of the fraction of the total current drawn from each supply port range from 20.39% (for V_{DD10}) to 38.04% (for V_{DD2}). An interesting feature to note are the higher peaks around the edges and the four corners of the grid. This occurs because the circuits in these regions see a different distribution of supply ports surrounding them than the circuits located near the middle of the CUT.

Figure 7(c), shows the hardware data shown in Figure 7(a) calibrated with the S1 simulation data shown in Figure 7(b). It is clear that the calibrated hardware data and the simulation data look very similar. The edge effects are also distinctly visible and the peaks are more uniform than the uncalibrated hardware measurements. Thus the calibration procedure has successfully removed the wide variations introduced by the non-uniform R_ps.

4.0 Look-Up Table Localization Algorithm

One benefit of using the calibration procedure is that it facilitates the implementation of a very simple Look-Up Table (LUT) based defect localization technique that exploits the regional signal behavior of the power grid. The calibrated multiple supply port current distribution contain valuable information about a defect's location in the layout and can be utilized for localization.

As previously indicated in Section 3.4, in the absence of process variability and grid modelling inaccuracies, the transformed data should exactly match the simulation data. However, since no two chips are identical and our simulation model grid was constructed using only the nominal parameters specified by the technology, the transformed hardware data differ from the simulation data. A reliable LUT based procedure is still possible by adopting an algorithm based on a 'fuzzy' match criteria. In the LUT based algorithm, we try to find a CPV stored in the database that bears the closest resemblance to the calibrated test CPV. Recall that a CPV is an ordered list of normalized multiple supply port current measurements in the sequence (I_{VDD0}, I_{VDD1}, ...I_{VDD20}) for any given location. The metric chosen to determine a fuzzy match is the minimum of the sum of

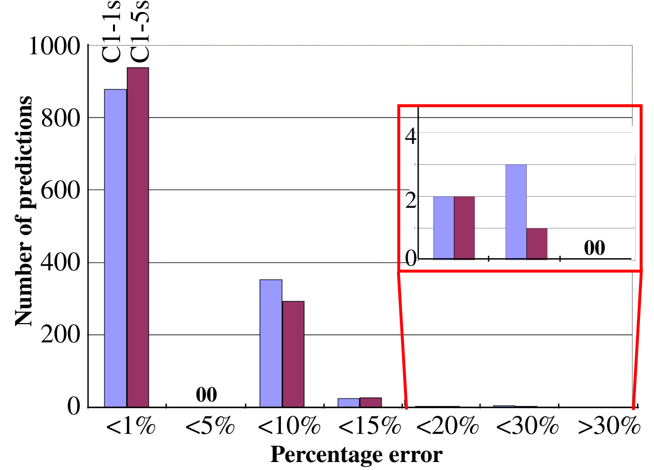


Figure 8. Chip 1 prediction results for C1-1s and C1-5s models.

all the point wise absolute differences between the test CPV and the CPVs stored in the database computed over all (x,y) locations. Equation 5 gives the criteria for a CPV

$$match = min\left(\forall(x, y)\sum abs(CPV_{test} - CPV_{x, y})\right) \quad \text{(Eq. 5)}$$

match.

In the above expression, CPV_{test} represents the calibrated test CPV obtained under a logic test and $CPV_{x,y}$ represents the simulated CPVs. We also explored some other metrics like minimum sum of the squared differences between the test and database CPVs and waveform correlation. However, the metric of Equation 5 yields the best results.

5.0 Experimental Results

We evaluated the LUT based defect localization method on 9 copies of the hardware CUT described in Section 3.1. Several parameters of the experimental space were analyzed and are first presented in Sections 5.1 through 5.3. The results of applying the LUT algorithm to the CUTs are presented in Section 5.4.

5.1 Noise Analysis

One of the first parameters of the experimental space that we studied was the effect of noise in our experiments. In order to analyze the effect of noise, we collected two data sets for the first chip (chip 1). The first data set was collected by sampling only one current value whereas the second data set used an average of five samples. Figure 8 shows the distribution of prediction errors for chip 1 one-sample (**C1-1s**) and five-sample (**C1-5s**) data, both calibrated with the S1 simulation model. The y-axis represents the number of predictions within the error ranges indicated

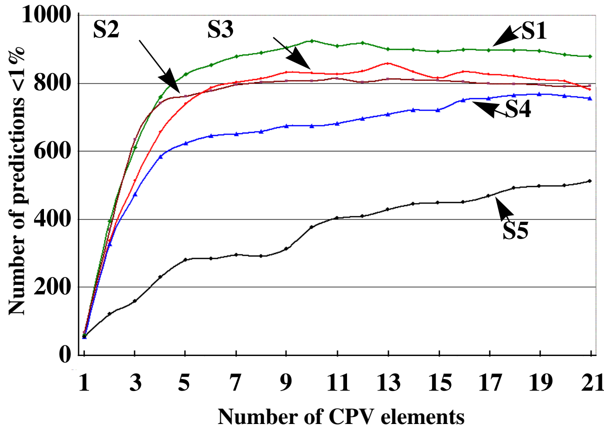


Figure 9. Predictions with less than 1% error for chip 1 calibrated to all 5 simulation models vs. number of CPV elements.

on the x-axis. The error is computed by taking the euclidean distance between the actual and the predicted locations and expressed as a percentage of the length of the diagonal of a quad as depicted by the dotted line in Figure 1. The expression used for computing the error is shown in Equation 6.

$$\%\ \text{err} = \frac{\sqrt{(x_{actual} - x_{pred})^2 + (y_{actual} - y_{pred})^2}}{l_{diagonal}} \times 100 \quad \text{(Eq. 6)}$$

In Equation 6, (x_{actual}, y_{actual}) represent the coordinates of the actual test circuit location, (x_{pred}, y_{pred}) represent the coordinates of the predicted location and $l_{diagonal}$ represents the length of the diagonal of a quad (computed to be 2086 units)[1].

The bar on the left in Figure 8 (labelled **C1-1s**) represents the data with only one-sample measurement and the bar on the right (labelled **C1-5s**) represents the five-sample measurement. It is clear from Figure 8, that averaging over 5 samples yields marginally better prediction results than the 1 sample counterpart. This is expected because averaging a data set tends to cancel out random measurement noise. However, the marginal improvement does not justify the increased test time. Therefore only one data sample was collected for the remaining 8 CUTs.

5.2 CPV Significant Element Analysis

In this section, we present results to evaluate an optimal number of significant elements of the CPV (i.e. elements with the highest magnitudes) necessary for accurate prediction. As mentioned before, due to the regional isolation provided by the power grid, the defect draws the greatest fraction of its current from the supply ports that are in close proximity. The current measurements from supply ports that are far off have a smaller, possibly negative, contribution in Equation 5 because of the reduced signal-to-noise ratio. Therefore, better results may be obtained using only a subset of the 21 elements in the CPVs in the matching algorithm.

The plot in Figure 9 shows the effect of considering different number of significant CPV elements on the prediction accuracy. The x-axis in Figure 9 represents the number of CPV elements used in Equation 5 for finding the closest matching CPV and the y-axis represents the number of predictions with <1% error. Each of the five curves in Figure 9 represent a different simulation model that was used to calibrate the chip 1 data. For example, the curve labeled S1 represents predictions from chip 1 calibrated using the S1 simulation model.

The low values on the left of Figure 9 indicates that considering too few CPV elements lead to bad prediction accuracy for all 5 models. The optimal value is between 10 and 12 CPV elements for the S1 curve. This is a reasonable expectation given the grid topology and tap point configuration shown in Figure 1. We used the highest 10 CPV elements in our analysis of the remaining 8 CUTs.

5.3 Calibration Model Analysis

The last element that we explore in this work is the impact of the simulated probe resistance on the calibration method and prediction accuracy of the LUT method. As indicated, we constructed five different probe resistance models namely S1, S2, S3, S4 and S5. From Figure 9, it is clear that amongst the 5 simulation models, the best prediction results are obtained by using S1 which is the 1 Ω uniform R_p model. Nearly 73% (924 out of 1260) of the predictions are correct when model S1 and the 10 most significant CPV elements are used for the analysis of chip 1. The results in Figure 9 also indicate that the optimal model is between 1 mΩ and 8.77 Ω. It is interesting to note that calibrating using a non-uniform R_p model (S5) yields poor results even though the model is a closer match to the CUT. This suggests that best results are likely to be obtained by calibrating using a uniform R_p model.

5.4 Generalized LUT algorithm

The complete error analysis for chip 1 using the S1 model and the highest 10 CPV elements is shown by the leftmost bars in Figure 10. In the analysis, 1134 of the 1260 predictions have less than 10% error. However, there are still 23 predictions with errors between 10% and 15%, 1 between 15% and 20% and 2 between 20% and 30% as

1.Although the prediction error for the leftmost bar is given as <1%, the uncertainty of the prediction in this group is bounded by approximately 5%, which corresponds to half the width of each test circuit.

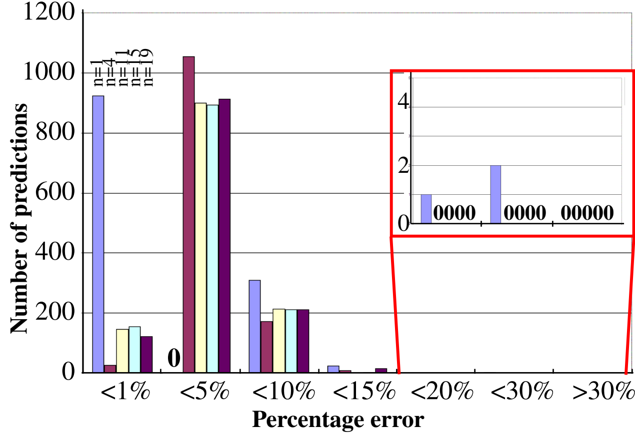


Figure 10. Prediction results for chip 1 calibrated to S1 model using 10 CPV elements for 5 different 'n' values.

shown in the figure. This sets the highest error bound between 20% and 30% for the LUT method. This section examines a variation of the LUT algorithm designed to reduce the maximum error bound at the expense of increasing the level of error in the good predictions.

Recall that the fuzzy match criteria discussed in Section 4.0 used the closest database $CPV_{x,y}$ match to the test CPV (CPV_{test}). Due to noise in the measurements, it is conceivable that the actual test circuit location is given by the second closest CPV match rather than the closest match. In such a situation, a weighted average of the locations predicted by the first two closest CPV matches is likely to yield better prediction results. This idea can be extended to using an average of 'n' closest CPV matches. The weights used to multiply the ordered set of predictions are given by '1/n' where 'n' represents the index of the nth closest match. For example, the location predicted by the closest CPV match corresponds to n=1 and hence has a weight of 1, the location predicted by the second closest match corresponds to n=2 and has a weight of 1/2 etc. Note that for n=1, the algorithm described in this section is equivalent to the basic LUT algorithm outlined in Section 4.0. Thus this algorithm is a more generic version of the basic LUT method.

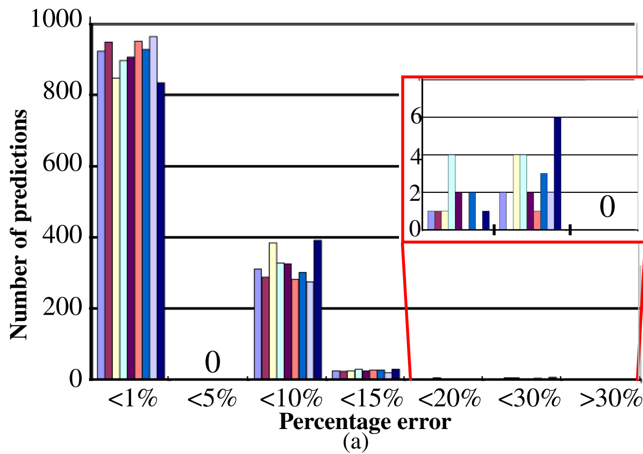
5.4.1 Optimal value for 'n'

In this section we evaluate an optimal value of 'n' necessary to reduce the highest error bound. The plot in Figure 10 shows the prediction error distribution for 5 different values of n (1, 4, 11, 15 and 19). The y-axis in Figure 10 represents the number of predictions within the error ranges indicated on the x-axis. The left most bar in Figure 10 corresponds to n=1 and right most n=19. The zeroes indicate that there were no predictions in that category. It is clear from Figure 10 that using an average corresponding to n=11 yields nearly 99% of the predictions with error less than 10%. Only 1 out of 1260 predictions has an error between 10% and 15%. The drawback of this approach is that the number of predictions with less than 1% error are reduced because the final predicted location is computed from an average of the *n* closest predictions. For example, the n=11 analysis gives the number of predictions with less than 1% error as 146, which is smaller than 924 for n=1. To exploit the best of both methods, an optimal strategy is therefore to use both algorithms. First the basic LUT algorithm is applied. If the defect is not located within this region, the region surrounding the point predicted by the generalized LUT is searched.

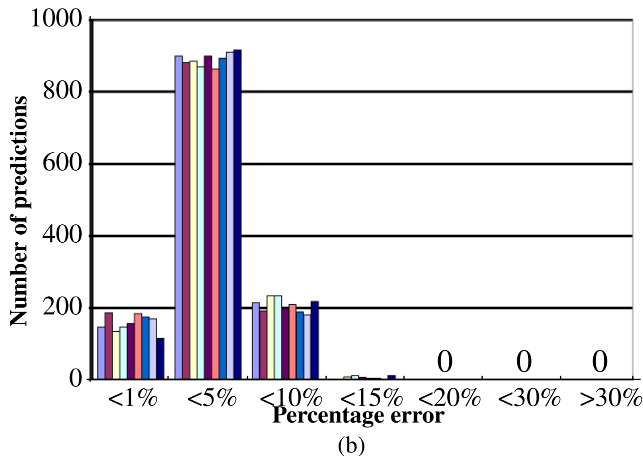
Figure 11 shows the prediction error distribution for the remaining 8 chips. These 8 chips have been calibrated to the S1 simulation model and the prediction results shown correspond to 10 CPV elements. Figure 11(a) shows the predictions results obtained by applying the basic LUT algorithm and the Figure 11(b) shows the results obtained by applying the generalized LUT algorithm for n=11. Results of the first chip are also repeated here for purposes of comparison. The left most bar in Figure 11 represents chip 1 and the right most bar represents chip 9 with all the other chips shown in between. The inset in Figure 11(a) shows a zoomed in view of the bins greater than 15% error. Results for all the 9 chips are similar. For n=1, number of predictions with error less than 1% are high but the number of predictions with error greater than 15% are non zero. However, Figure 11(b) shows that using n=11 limits the maximum error bound to less than 15% at the expense of the number of predictions with errors less than 1%. An interesting feature to note is that for n=1, there were no predictions with errors between 1% and 5%. This is true because of the discrete number of test circuits on the chip. However, using n=11 reduces the number of predictions with less than 1% error but increases the number of predictions with errors between 1% and 5%. This is an artifact of averaging the 11 predicted locations. A large fraction of the predictions with error less than 1% are now transferred into the <5% bin.

6.0 Conclusions

In this paper we explored the possibilities of defect localization using power supply signals. We conducted hardware experiments to corroborate our simulation results. Hardware experiments show that the power grid indeed creates regional behavior that can be used for defect localization purposes. We also demonstrated a powerful calibration procedure that enables us to compensate for test equipment/environment variabilities by transforming the highly skewed hardware data into a more balanced data set that we used to implement a LUT based defect localization technique. We also introduced two variations of the LUT based



(a)



(b)

Figure 11. Prediction results for 9 chips.

localization algorithm and demonstrated the accuracy of each by performing localization on nine copies of the test chip.

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