Digital Integrated Circuit Testing using Transient Signal Analysis

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Abstract

A novel approach to testing CMOS digital circuits is presented that is based on an analysis of I_{DD} switching transients on the supply rails and voltage transients at selected test points. We present simulation and hardware experiments which show distinguishable characteristics between the transient waveforms of defective and non-defective devices. These variations are shown to exist for CMOS open drain and bridging defects, located both on and off of a sensitized path.

1.0 Introduction

Transient Signal Analysis (TSA) is a new parametric testing method for digital integrated circuits. In TSA, transients in both the voltage waveforms at selected test points as well as current transients on the power supply are analyzed to determine the presence of defects. TSA exploits the fact that the power supply is globally connected to a large fraction of the transistors in a CMOS digital integrated circuit. TSA is similar to power supply current (I_{DD}) test methods in this way. Since power supply connections are unbuffered at the I/O pads, it is possible to measure the high frequency components of this signal without attenuation. Thus, the I_{DD} transients reflect the switching activity associated with the propagation of signals throughout the circuit. However, in larger circuits, the number of transistors which can simultaneously switch often makes it difficult to identify a defect using this single resource. TSA improves on defect detection capabilities of I_{DD} test strategies by additionally monitoring the voltage transients at a set of test points as well as on I_{DD}. The voltage test points are typically at or near the primary outputs of the device. By using a combination of voltage transients on test signal paths and I_{DD} transients on the power supply, TSA can provide improved defect resolution while maintaining a high degree of process insensitivity when compared with other I_{DD}-based testing methods.

In this paper, we present results from four experiments conducted on actual devices with intentionally inserted bridging and open drain defects. In order to demonstrate the sensitivity advantage of TSA over logic testing, we have placed several bridging and open drain defects into separate versions of a test circuit and have conducted experiments using two-vector test sequences that do not generate logic errors at the test points. The results presented for the experiments show regional variations in the test point signals due to the presence of the defects.

The remainder of this paper is organized as follows. In Section 2 we present related research on device testing and the motivation for our research. Section 3 presents the results of hardware experiments conducted on devices with intentionally inserted bridging and open drain defects. Section 4 gives a summary and conclusions.

2.0 Background and Motivation

Device *logic testing* analyzes the logical integrity of the device by using input test vectors which are a subset of all possible stimuli. However, these subsets are generated by techniques which are based on fault models that have been shown to be inadequate to detect all forms of CMOS defects [1][2]. *Parametric testing* strategies [3][4], on the other hand, are based on the analysis of a circuit's parametric properties, for example, propagation delay, magnitude of supply current or transient response. While the algorithms for generating logic tests have been improved over time to handle more types of fault behaviors, parametric testing strategies offer intrinsically better solutions since they have been developed from the structural and electrical properties of CMOS circuits.

There are many types of parametric tests that have been proposed [5]. Recent research interest has focused primarily on three types; I_{DDQ} [6], I_{DD} [7], and delay fault testing [8][9]. I_{DDQ} is based on the measurement of an IC's supply current when all nodes have stabilized to a quiescent value [10]. I_{DDQ} has been shown to be an effective diagnostic technique for CMOS bridging defects, but is of limited applicability for some types of CMOS open defects [11]. Although defect observability is significantly improved by the addition of I_{DDQ} to logic tests, I_{DDQ} is handicapped by the necessarily slow test vector application rates, the limited resolution achievable for large ICs and the restricted class of CMOS circuits to which it is applicable.

Several dynamic supply current I_{DD}-based approaches

have since been proposed to overcome the limitations caused by the static nature of the I_{DDQ} test. Frenzel and Marinos [7] proposed an I_{DD}-based method in which sinusoidal waveforms are used as the input stimulus and defect detection is accomplished by comparing the number and position of the current pulse transitions across the mean current value with those of a defect-free device. Hashizume, *et al.* [12] analyzed the frequency spectrum of the I_{DD} waveform as randomly selected test vectors were applied to a circuit. Dorey, *et al.* [13] evaluated the I_{DD} test (and other parametric methods) as a reliability measure of a device. Beasley, *et al.* [14] have proposed an I_{DD} technique that uses neural networks to analyze the I_{DD} waveform that results from pulsing the power and ground supplies. Thibeault [15] proposed a defect detection method that uses the first harmonic to estimate the frequency spectrum of the current and output voltage waveforms. Makki, *et al.* [16] have proposed an I_{DD} test that thresholds the I_{DD} transient generated by isolated transistor pseudo-partitions in order to accomplish defect detection. In general, these I_{DD}-based methods are not hampered by the slow test application rates and are not as sensitive to design styles as I_{DDQ}, however, circuit size and topology are still factors that affect the defect resolution of these schemes. Also, these methods do not provide a means of accounting for changes due to normal process fluctuations and are therefore subject to aliasing problems.

Alternatively, delay fault testing takes advantage of the fact that many CMOS defects cause a change in the propagation delay of signals along sensitized paths [2]. Since the test is dynamic and regional, delay fault testing does not suffer from slow test vector application rates, as is true of I_{DDQ}, and is not as sensitive to circuit size, like I_{DD}. More recently, Franco and McCluskey [17] proposed two extensions to delay fault testing in which the outputs are monitored continuously before and after the sampling event. Chatterjee, *et al.* [18] discussed a similar output waveform integration method for the detection of stuck-at failures. And Wu, *et al.* [19] proposed a testing method for analog devices that uses a neural network to analyze the shape of the output signals of the device. One of the difficulties with delay fault testing is that test vector generation is complicated due to static and dynamic hazards [20]. Also, since the number of possible paths in a circuit is much larger than the number of paths that are typically tested, the effectiveness of a delay fault test is dependent on the propagation delay of the tested paths and the delay defect size, for path delay fault testing, and the accuracy of the test equipment, for gate delay fault testing[21]. Lastly, Pierzynska and Pilarski [22] have shown that a non-robust test can detect a delay fault undetectable by any robust test.

Recently, Ma, *et al.* [23] and others[1][2][24][25] evaluated a large number of test methodologies and determined that a combination of several test strategies may be necessary in order to find all defective devices. In particular, Ma, *et al.* discovered that I_{DDQ} cannot detect all kinds of defects and must be used with some kind of dynamic voltage test. Our technique, Transient Signal Analysis (TSA), with its advantages in defect detection and process insensitivity, is proposed as an addition to this test suite.

TSA is based on a measurement of the contribution to the transient response of a device by physical characteristics such as substrate, power supply or parasitic coupling which are present in any circuit. In previous papers [26][27], we have demonstrated through simulation experiments that global variations of major device performance parameters, i.e. threshold voltage and gate oxide thickness, result in measurable changes of the circuit's transient response at all test points. In contrast, the presence of a device defect will change both the value and topology of the parasitic components in the region of the defect. For example, a single open circuit for the connection to the drain terminal of a CMOS transistor will remove a percentage of the normal parasitic capacitance present on the output node of the associated logic gate. Similarly, a bridging short between two or more gate output lines will add new parasitic resistive and capacitive elements at each of the shorted nodes. We have shown through other simulation experiments that the changes introduced by both of these classes of defects result in measurable variations in the transient response and that these variations are distinct at two or more test points.

By analyzing the transients at multiple test points and assuming process variation is uniform across individual die, TSA is able to distinguish between the changes in the transient response caused by defects and those caused by process variation. This is true because, in the latter case, the transients generated at each of the test points will be correlated in the defect-free device. On the other hand, the presence of a defect will have a larger influence on the transients at test points closer to the defect. Therefore, defect detection is accomplished in TSA by analyzing the transients at all test points simultaneously so that global process variations can be distinguished from the regional defect variations.

3.0 Experiments

In this section we present the results of several experiments designed to demonstrate that it is possible to capture the important frequency components of the transient response at the test points. We also show that these signals can be used to distinguish between defective and non-defective devices by demonstrating that signal variations caused by defects couple across parasitic components and are measurable on nodes topologically close to but not sen-

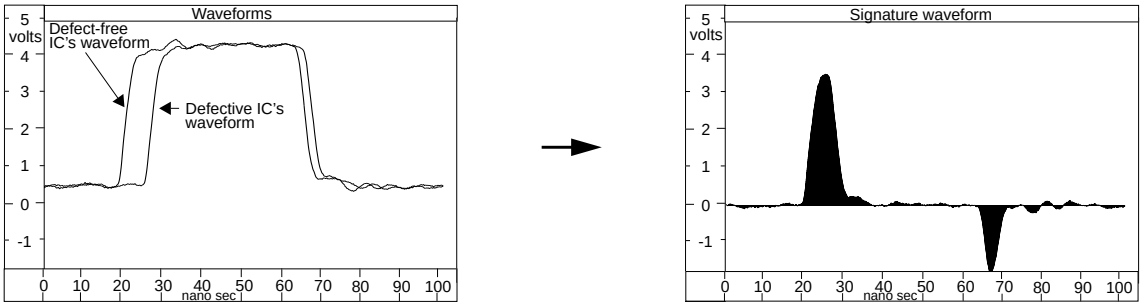

Figure 1. Waveforms from two devices (left), and their Signature Waveforms (SW) (right).

sitized from the defect site.

We have first simulated and then fabricated four copies of three versions of a test circuit (twelve ICs total), a version with intentionally inserted bridging defects, a version with intentionally inserted open drain defects and a defect free version. The defect locations were selected so that they could be examined with minimal interaction. This required that the sensitized paths disrupted by each of the defects be both logically disjoint and topologically distant. The latter requirement additionally provides the ability to test on paths which are not sensitized through the defect but are topologically nearby in the layout. Additionally, the use of simulations allowed us to manipulate the circuit model to identify the key components contributing to the observed behavior of the transients generated in the actual devices.

For these experiments, we used the ISCAS85 c432 benchmark circuit [28]. The circuit was synthesized with OCTTOOLS using the ITD/AμE SCMOS standard-cell library. Four copies of each version of the test devices were fabricated by MOSIS using ORBIT's 2.0μm SCNA process. The defect-free versions were verified using both functional and Stuck-At test sets. The simulation models were created using the MAGIC circuit extractor and were configured using simulation model parameters returned from the fabrication runs. The simulation experiments were conducted using SPICE.

The TSA testing process involves applying a test vector sequence to the primary inputs (PIs) of an IC and sampling the waveforms generated in both I_{DD} and a set of primary outputs (POs). As an example, the plot shown on the left of Figure 1 is a waveform collected from a primary output of two devices. The difference waveform is shown on the right, shaded along a zero baseline as a means of emphasizing the differences in the waveforms. We refer to the difference waveform as a **Signature Waveform** (**SW**).

In our experiments, a 1 GHz channel of a digitizing oscilloscope is used to collect a 2048 point waveform (1 point every 50ps). The minimum sampling interval of the oscilloscope is 50ns, therefore 1000 repetitions of the two vector sequence is required in order to build the waveform. The averaging function of the oscilloscope is used to average 32 complete samples of the waveform before it is saved in order to reduce ambient noise levels. These waveforms are subsequently passed through a low-pass filter to reduce RF noise (above 250MHz). The experiments were run at 11 MHz, about half the maximum frequency of the devices.

The test points for these experiments are the seven primarily outputs and the V_{DD} supply input of the test devices. The I_{DD} transient was measured differentially across a 10 Ohm resistor while the voltage transients were measured directly from the I/O pads. In each experiment four non-defective and four defective devices were tested. One of the non-defective devices was chosen as a standard. Simulation data of modeled defect-free and defective circuits were also generated for points both before and after the MOSIS SCN20 I/O pads. This was done to estimate the degree of high frequency attenuation introduced by the I/O pads used in the ICs. As shown below, in general, the simulations were conservative with respect to the measured data. Further, we expect the response characteristics of industry pads to be much better since there is a significant performance gain achievable by making them unidirectional and optimizing their response characteristics.

3.1 Bridging Experiments

First we report on two bridging defect experiments. We have specifically selected the test vector sequences so that no logic error is produced at any of the POs. The first experiment illustrates the invalidation immunity of a TSA test to static hazards while simultaneously demonstrating the defect's presence directly. It is important to note that the emphasis of this experiment and the open drain experiment discussed in the next section is on the coupling of the hazard signal changes to the other primary outputs and not on its direct observation at the POs. The second experiment shows the detection capability of TSA for bridging defects that change the delay characteristics of sensitized paths but do not produce logic errors at the primary outputs. Both sets of results show the regional signal variations created by the presence of the defect.

3.1.1 Bridging Experiment 1

Figure 2 shows a portion of the schematic diagram of the c432. Only those sensitized paths affected by the defect

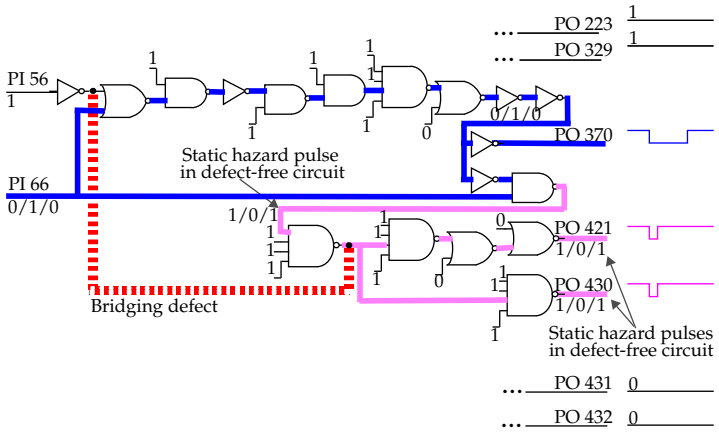

Figure 2. Portions of the c432 showing the short and the sensitized paths affected by defect of Bridging Exp. 1.

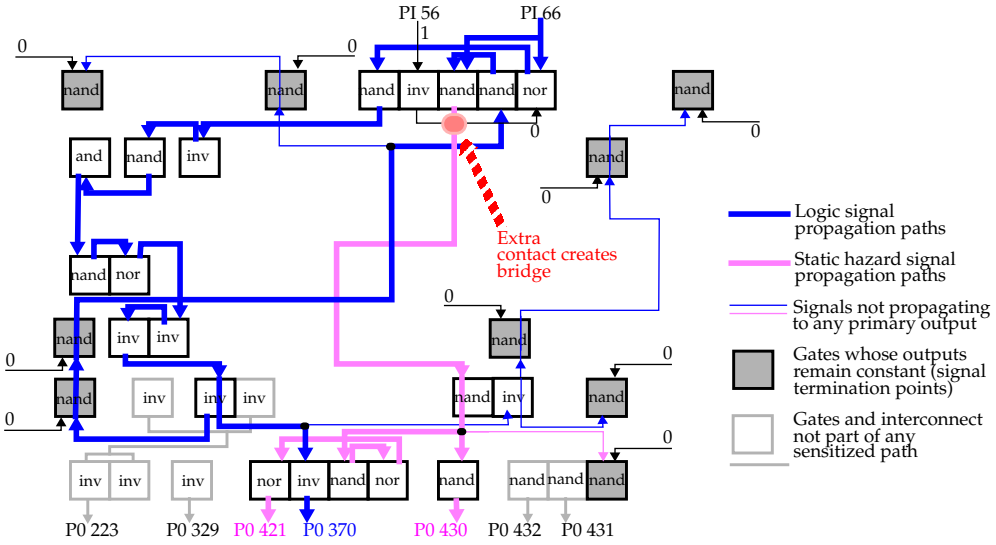

Figure 3. Portions of the c432 layout showing spatial relationship of the std cells along sensitized paths of Figure 2.

are shown. The input stimulus for this experiment toggles PI 66. PI 56 is held high and the other PIs (not shown) are held low. The red dotted line in the figure represents the bridging defect which was created in the layout by inserting a first-level to second-level metal contact between the output lines of a 4-input NAND gate and an inverter as shown in Figure 3. This simulates an SiO_2 defect. The only PO that changes logic state is 370. However, in the defect-free circuit, a static hazard causes a pulse to propagate to POs 421 and 430 along paths shown in magenta in the figure. Note that the bridging defect is not on any sensitized path and no contention exists between the two bridged nodes in steady-state. However, since the output of the inverter driven by PI 56 is low, the bridge eliminates the pulse produced by the hazard in the defective circuit.

Figure 3 shows the spatial relationships of all sensitized paths in a portion of the c432's layout. Gates with no outputs are shaded gray and indicate the termination of signal propagation. For clarity, non-dominant inputs to the gates are not shown. Paths shown with thick blue lines correspond to the paths shown in blue in Figure 2. The thin blue lines are sensitized paths which terminate at internal gates and are not shown in Figure 2. A similar relationship exists for the magenta lines in both figures. The bridging defect is shown in the figure as a shaded red circle. The lightly shaded gates shown along the bottom of the figure remain at DC values in this experiment. Some of the driving gates for PO 223 are shown to illustrate the potential for signal coupling between the DC outputs and the sensitized paths. Similar types of coupling exist for POs 329, 432 and 431.

Each of the plots in Figure 4 shows a set of SWs from a single PO or I_{DD} test point. The top-most waveform of each plot is the output trace from the standard IC used in the difference operation to create the SWs shown below it. The next three waveforms labeled DF#*x* (colored dark-green) are the SWs from each of the three *Defect-Free* ICs. The next four SWs, labeled either BR#*x* for *BRidging*

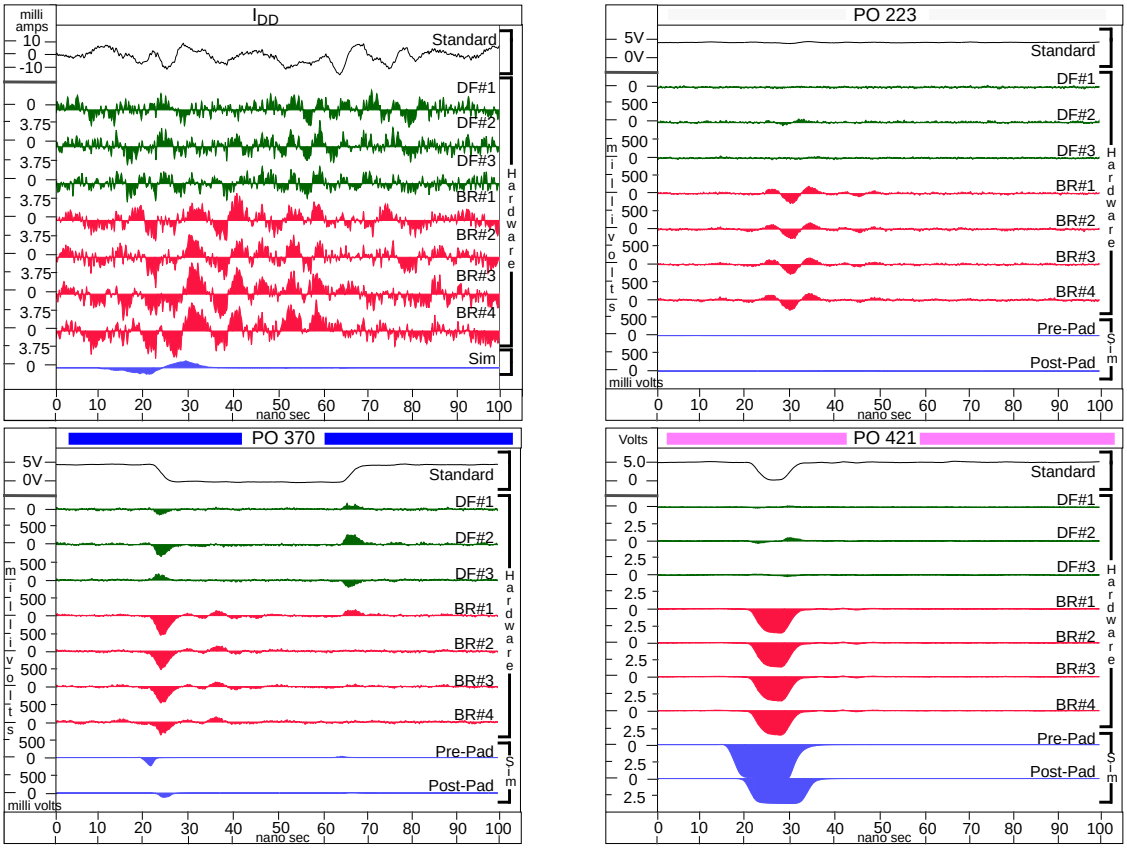

Figure 4. I_{DD}, PO 223, 370 and 421 SWs from Bridging Experiment 1.

defects or OD#*x* for *Open Drain* defects (colored red) are the difference waveforms from the four defective ICs. The bottom two waveforms (colored blue) represent the Pre-Pad and Post-Pad SWs from the corresponding simulation. The I_{DD} figures show only one simulation result since there are no pad drivers for these pads.

The top-left plot of Figure 4 shows the I_{DD} SWs produced from this experiment. There is clearly a variation in the current waveforms in the 15-40 ns time range corresponding to the removal of the static hazard. The top-right plot of Figure 4 shows the SWs generated on PO 223. The defect causes a distinctive transient to be generated in all four of the BR#x SWs of this PO. Since the simulation SWs do not agree with these results, we know that in this case our simulation model does not capture the source of this coupling. This may be due to inaccuracies in modeling the parasitics either in the core logic or in the power supply rails of the I/O pads or both. Similar types of transients also appear in the SWs of POs 329, 431 and 432.

The bottom-left plot of Figure 4 shows the SWs generated on PO 370. Like PO 223, this PO is not on a sensitized path with the bridging defect. However, unlike PO 223, the Pre-Pad and Post-Pad simulation results show transients in this region of the SWs. In fact, since the transients appear in the Pre-Pad results, we hypothesize that the transients in the BR#x SWs of this PO are not due to the transients generated in the power supply lines of the pads. Moreover, since the simulation model was derived without any resistance between the core logic power supply and the sources of the transistors, coupling through the common power supply lines of the core logic can also be eliminated as the only source. Therefore, we can conclude that at least part of this variation is due to capacitance coupling between nodes in the core logic.

The bottom-right plot of Figure 4 shows the SWs generated on PO 421. The SWs generated on PO 430 are similar. As noted above, the bridge ‘shorts out’ the pulse created by a static hazard in the defect-free circuit. This clearly shows up in the defective SWs since a defect-free waveform is used as the reference.

3.1.2 Bridging Experiment 2

Figure 5 shows a portion of the c432 schematic with the sensitized paths for the second bridging experiment. PI 69 is toggled while PI 82 is held high. All other PIs are held low. PO 432 is the only output that changes state in this experiment. Unlike the previous bridging experiment, the defect is on the sensitized path driving PO 432. Again, no contention exists between the two bridged nodes in steady-

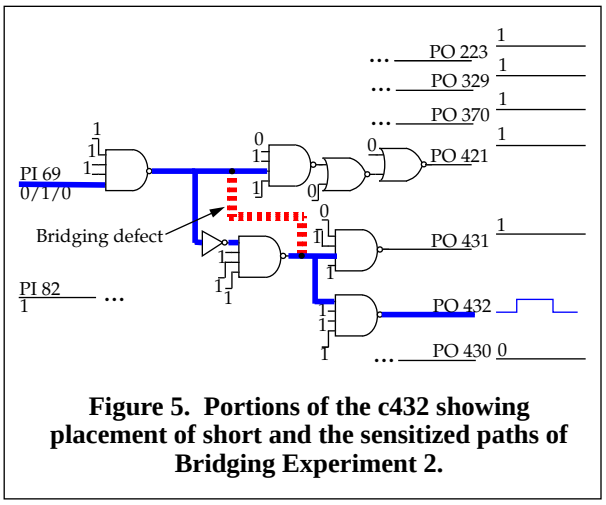

Figure 5. Portions of the c432 showing placement of short and the sensitized paths of Bridging Experiment 2.

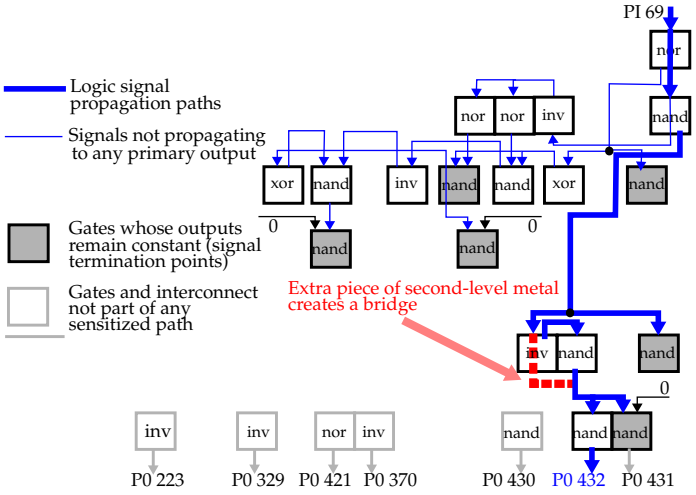

Figure 6. Portions of the c432 layout showing spatial relationship of std cells along sensitized paths of Figure 5.

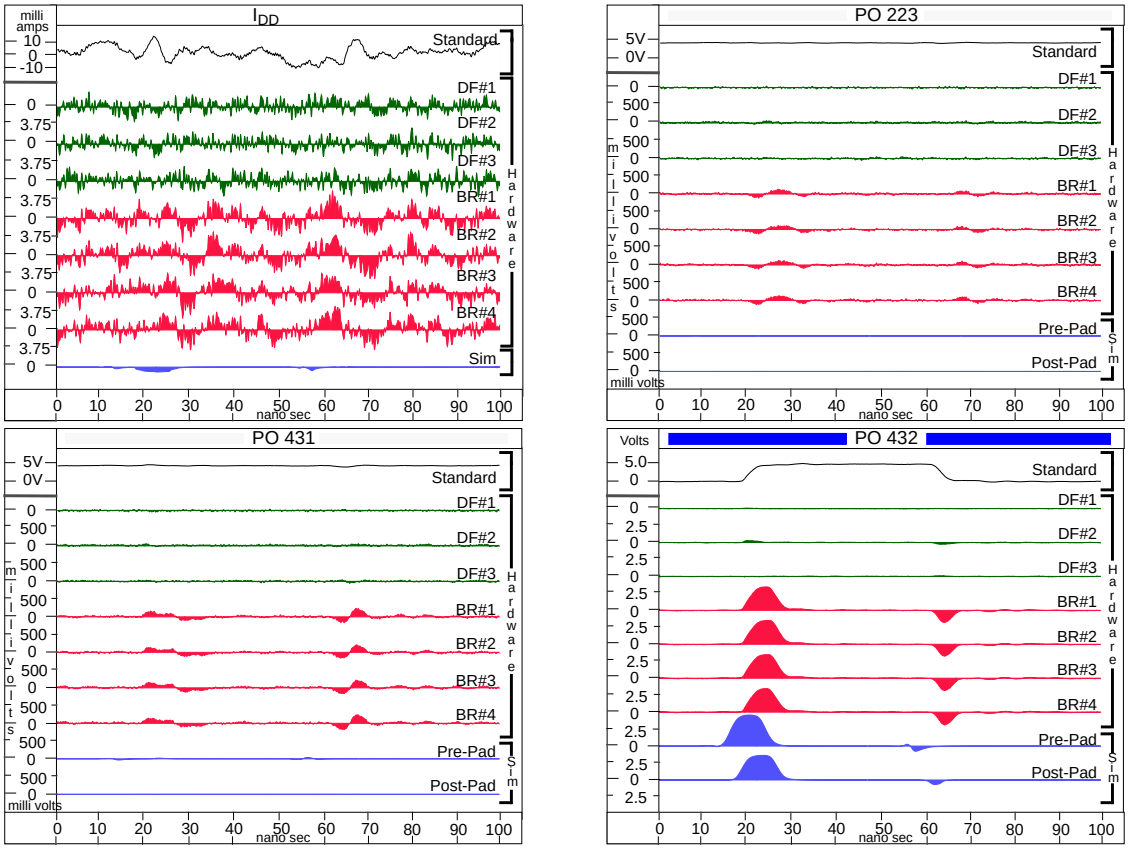

Figure 7. I_{DD}, PO 223, 431 and 432 SWs from Bridging Experiment 2.

state and the circuit operates logically correctly under this test sequence. Figure 6 shows the spatial relationships of the sensitized paths for the second bridging experiment. The bridging defect is shown in the figure as a red dotted line but is physically represented as an extra piece of second-level metal between the outputs of two 4-input NAND gates.

The top-left of Figure 7 shows the I_{DD} SWs. As in the previous experiment, transients in the I_{DD} SWs correlate in time (at about 25 and 65ns) with observed changes in the POs. The top-right plot of Figure 7 shows the SWs generated on PO 223. The same type of pattern exists for POs 329, 370, 421 and 430. Some type of coupling is occurring but, as in the first bridging experiment, we can not deter-

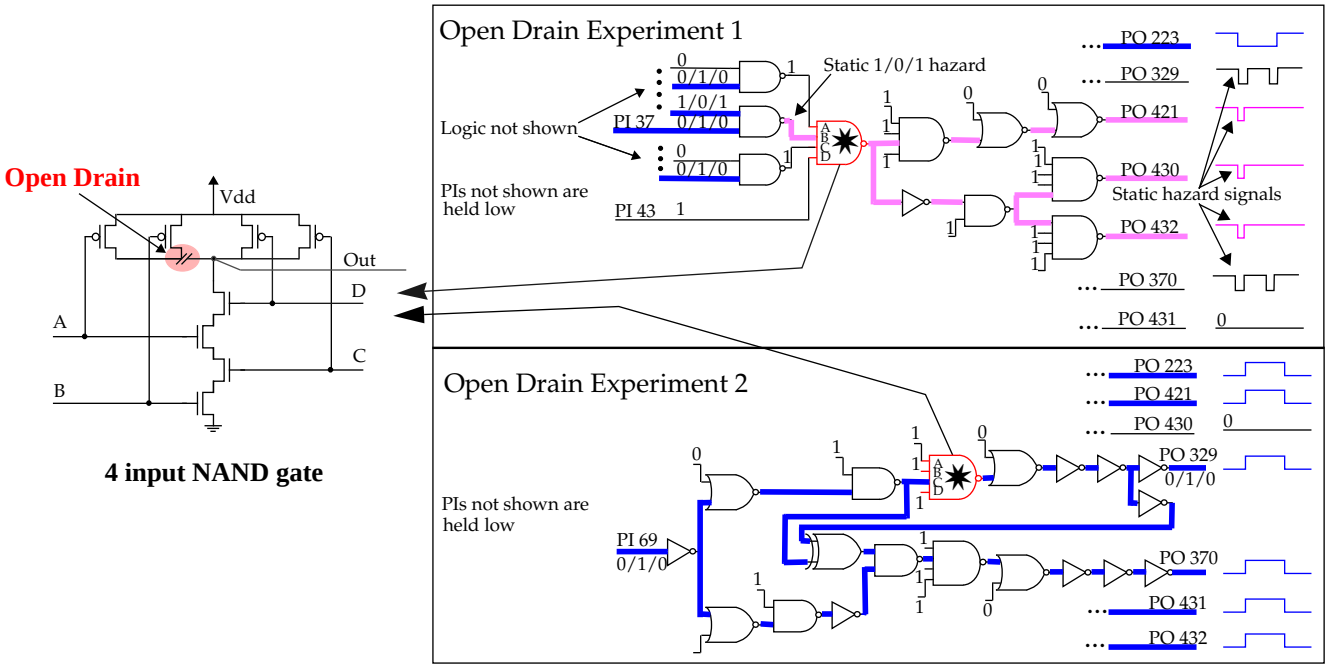

Figure 8. Portions of the c432 showing the sensitized paths from the open drain defects.

mine the source using our simulation model. The bottom-left plot of Figure 7 shows the SWs generated on PO 431. The transients are unique to this PO and may be the result of coupling that occurs through the gate oxide of the 4-input NAND driving this PO. The pre-pad simulation SWs support this conjecture. The bottom-right portion of Figure 7 clearly shows the delay introduced by the defect on PO 432 in both the simulations and the hardware. This is the best example of the advantages in TSA of continuously monitoring the POs. We now turn to more difficult detection task of open drain defects.

3.2 Open Drain Experiments

The results of two open drain experiments are presented in this section. Like the bridging experiments, we have selected the test vector sequences so that no logic error is generated at any of the POs. The first experiment is similar to the first bridging experiment in that the signals from static hazards are exploited for defect detection. The test sequence selected for the second experiment is designed to test the change in loading capacitance caused by the defect and in this sense represents a harder defect detection experiment. The results of the experiment also serve to illustrate how process variations can affect defect detection when the change in the transient response is minimal.

Figure 8 shows the sensitized paths through the defective gates for the open drain experiments. The left side of Figure 8 shows an open drain defect in the transistor-level schematic diagram of a 4-input NAND gate. A three micron wide piece of first-level metal has been removed between the p-transistor drain pairs. Both of the open drain experiments test this type of defect in two different NAND gates in the circuit. The input stimuli for the experiments is shown in the middle of the figure. The test sequence for the first experiment generates a number of pulses at the POs which are created by a static hazard. The difference in the signal arrival times on the inputs to the NAND driven by PI 37 cause the output of the gate to pulse low. For the second experiment, the loading capacitance on the output node of the NAND gate consists of 118FF drain, 40FF routing and 59FF driven-gate capacitance. The open circuit removes two drains for approximately 42 FF or 19% of the total.

3.2.1 Open Drain Experiment 1

The top-right plot of Figure 9 shows the SWs for PO 223. This PO is on a sensitized path from PI 37 but is not on a sensitized path from the defective NAND gate. The SWs highlight the differences in the propagation delay of signals driving this output. It is apparent that the delay characteristics of the DF#2 and OD#3 ICs are each unique within their groups. This same type of behavior is also present in the SWs produced on POs 329 and 370 (not shown). Unfortunately, the relationship between the ICs and the wafers on which they were fabricated could not be obtained. However, we suspect that at least some of the variation we see in the SWs is due to fluctuations in the fabrication process. More interestingly, the region labeled *characterizing transient* in the figure reveals other transient information that is consistent with the classification of these ICs as defect-free and defective.

The bottom-left plot of Figure 9 shows the SWs gener-

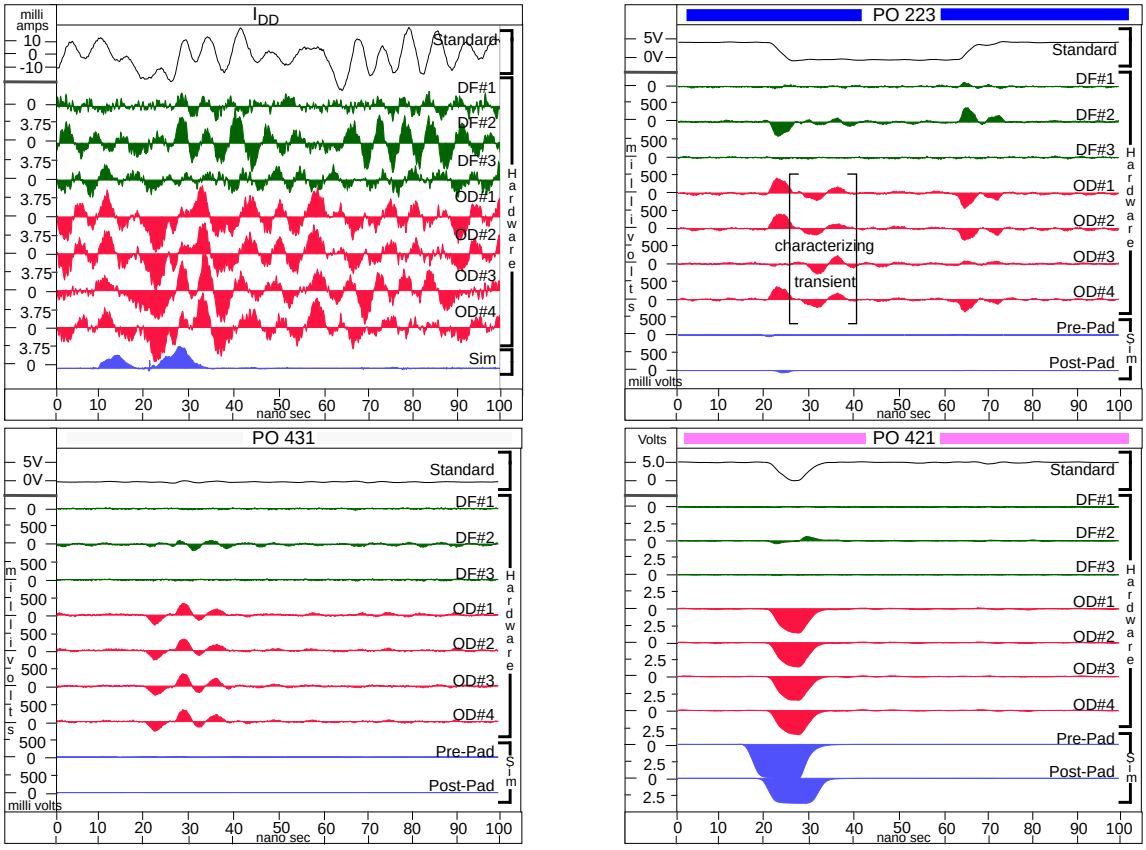

Figure 9. I_{DD}, PO 223, 431 and 421 SWs from Open Drain Experiment 1.

ated on PO 431. This output does not transition under the test sequence. However, the variations in the SWs provide a clear indication as to which group each of the ICs belong. The SWs of PO 421 shown on the bottom-right of Figure 9 also provide confirming information. By monitoring the output continuously, the defect can be detected since its presence eliminates the pulses normally produced by the static hazard. The SWs from POs 430 and 432 are not shown but are similar to PO 421. The IDD SWs are shown on the top-left of the figure. The correlation between these SWs and the SWs generated on the POs provide sufficient information to identify the defective ICs. These results show why we believe that by continuously monitoring the POs and correlating the effects among the POs we can differentiate between effects due to regional variations caused by defects and effects that are a result of process variation between different ICs.

3.2.2 Open Drain Experiment 2

The top-right plot of Figure 10 shows the SWs generated on PO 421 of the second open drain experiment. The SWs for POs 223, 431 and 432 are not shown since they are similar to these results. PO 421 is on a sensitized path from PI 69 but is not on a sensitized path from the defective NAND gate. Therefore, these SWs primarily illustrate variation in the process and/or variation in the pad circuitry. The classification of these devices as defective and defect-free is not clear based on these SWs.

The bottom plots of Figure 10 shows the SWs generated on POs 329 and 370 which are on sensitized paths from the defective NAND gate. The top-left plot of Figure 10 shows the I_{DD} SWs. Even though there is good correlation between these SWs and the corresponding SWs generated at the voltage test points for each of the ICs, there is less than expected correlation within each group (e.g., OD#3 and DF#2). Other tests of OD#3 show that the outputs from this IC were slower than the three other OD test ICs. Therefore, we believe that the change in the transient response caused by the defect's modification in the loading capacitance is not significant enough to be clearly observable at the POs given the amount of process variation present within the defective and defect-free IC groups. This signal variation may be attributable to inter-wafer process variation since MOSIS guarantees that the four identical copies of each device are fabricated on at least two different wafers.

4.0 Summary and Conclusions

The simulation and hardware experiments conducted on the c432 have shown that it is possible to capture the

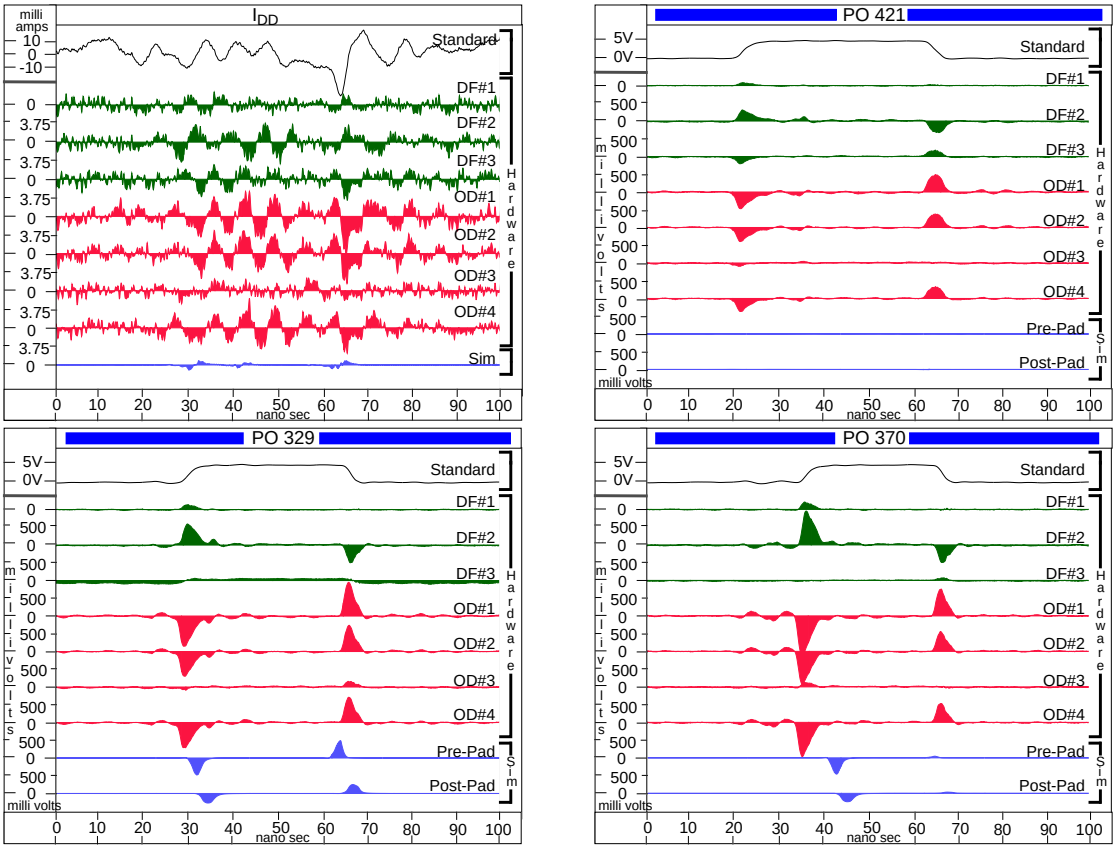

Figure 10. I_{DD}, PO 421, 329 and 370 SWs from Open Drain Experiment 2

important frequency components of the transient response. We have also demonstrated the existence of regional signal variations due to the presence of a defect, first in the bridging experiments and then in one of the open drain experiments.

For bridging defects, distinctive changes are observable on the I/O pads driven by POs that are not sensitized. This was shown on PO 223 in both bridging experiments and PO 431 in the second experiment. The same is true of open drain defects as shown for PO 431 in the first open drain experiment. This implies that the number of test vectors required to achieve a given fault coverage may be lower for TSA than for other testing strategies. This work also demonstrates that process variation can still make open drain defects difficult to detect under certain test sequences, as we illustrated with the second open drain experiment.

More importantly, however, the second open drain experiment illustrates that each of the test point signals are strongly correlated within each device. This attribute permits the use of a method based on the cross correlation of signature waveforms to help identify which variations are caused by process variation and which are due to defects. Consequently, the generation of a set of defect-free transient waveforms that take into account variations caused by normal process fluctuations becomes an important issue. The most straightforward approach of obtaining these waveforms would be to use a self-calibration method in which a set of defect-free reference devices, fabricated in the same lot as the test devices, are used to generate the expected set of transient waveforms. Another concern is the practicality of implementing this method for production test. Clearly, the methodology shifts the emphasis of the test to the back-end and redefines the data collection requirements of the test equipment but does not necessarily imply an increase in overall test cost. This will be true if it is determined that TSA can provide higher levels of quality with fewer test vectors.

We are currently conducting a set of on-chip probing experiments to verify the source of the transients observed in some of the results presented above and to evaluate the high frequency filtering properties of the I/O pads. More hardware experiments are planned to determine the detectability of gate oxide short defects and other types of opens and bridges.

We are also currently investigating a means of quantifying the degree of coupling through each of the main parasitic coupling mechanisms, namely, power supply,

internodal, well and substrate when defects are introduced into neighboring circuit components. This information and other simulation experiments will help us determine the number and position of the test points or the amount of observability required and subsequently, the number and type of test vectors necessary to achieve a given fault coverage and quality level improvement factor.

References

[1] Charles F. Hawkins, Jerry M. Soden, Alan W. Righter and Joel Ferguson. Defect Classes - An Overdue Paradigm for CMOS IC Testing. In *International Test Conference*, pages 413-425, 1994.

[2] Jerry M. Soden and Charles F. Hawkins. Electrical properties and detection methods for CMOS IC defects. In *Proceeding of the European Test Conference*, pages 159–167, 1989.

[3] Mark W. Levi. CMOS is Most Testable. In *IEEE Test Conference*, pages 217-220, 1981.

[4] F. Joel Ferguson, Martin Taylor and Tracy Larrabee. Testing for Parametric Faults in Static CMOS Circuits. In *International Test Conference*, pages 436-443, 1990.

[5] A. P. Dorey, B. K. Jones, A. M. D. Richardson, and Y. Z. Xu. *Rapid Reliability Assessment of VLSICs*. Plenum Press, 1990.

[6] Thomas M. Storey and Wojciech Maly. CMOS bridging fault detection. In *International Test Conference*, pages 1123–1132, 1991.

[7] James F. Frenzel and Peter N. Marinos. Power supply current signature (PSCS) analysis: A new approach to system testing. In *International Test Conference*, pages 125–135, 1987.

[8] E. P. Hsieh, R. A. Rasmussen, L. J. Vidunas, and W. T. Davis. Delay test generation. In *Proceeding of the 14th Design Automation Conference*, pages 486–491, 1977.

[9] Chin Jen Lin. On delay fault testing in logic circuits. *IEEE Transactions on Computer-Aided Design*, CAD-6(5):694–703, September 1987.

[10] Steven D. McEuen. I_{DDQ} benefits. In *VLSI Test Symposium*, pages 285–290, 1991.

[11] Adit D. Singh, Haroon Rasheed, and Walter W. Weber. I_{DDQ} testing of CMOS opens: An experimental study. In *International Test Conference*, pages 479–489, 1995.

[12] M. Hashizume, K. Yamada, T. Tamesada, and M. Kawakami. Fault detection of combinatorial circuits based on supply current. In *International Test Conference*, pages 374–380, 1988.

[13] A. P. Dorey, B. K. Jones, A. M. Richardson, P. C. Russel, and Y. Z. Zu. Reliability testing by precise electrical measurement. In *International Test Conference*, pages 369–373, 1988.

[14] J. S. Beasley, H. Ramamurthy, J. Ramirez-Angulo, and M. DeYong. I_{DD} pulse response testing of analog and digital CMOS circuits. In *International Test Conference*, pages 626–634, 1993.

[15] C. Thibeault. Detection and location of faults and defects using digital signal processing. In *VLSI Test Symposium*, pages 262–267, 1995.

[16] Rafic Z. Makki, Shyang-Tai Su, and Troy Nagle. Transient power supply current testing of digital CMOS circuits. In *International Test Conference*, pages 892–901, 1995.

[17] Fiero Franco and Edward J. McCluskey. Delay testing of digital circuits by output waveform analysis. In *International Test Conference*, pages 798–807, 1991.

[18] A. Chatterjee, R. Jayabharathi, P. Pant and J. A. Abraham. Non-Robust Tests for Stuck-Fault Detection Using Signal Waveform Analysis: Feasibility and Advantages. In *VLSI Test Symposium*, pages 354-359, 1996.

[19] A. Wu, T. Lin, C. Tseng, and J. Meador. Neural network diagnosis of IC faults. In *VLSI Test Symposium*, pages 199–203, 1991.

[20] Ankan K. Pramanick and Sudhakar M. Reddy. On the detection of delay faults. In *International Test Conference*, pages 845–856, 1988.

[21] E. S. Park, M. R. Mercer, and T. W. Williams. Statistical delay fault coverage and defect level for delay faults. In *International Test Conference*, pages 492–499, 1988.

[22] Alicja Pierzynska and Slawomir Pilarski. Non-Robust versus Robust. In *International Test Conference*, pages 123-131, 1995.

[23] Siyad C. Ma, Piero Franco, and Edward J. McCluskey. An experimental chip to evaluate test techniques: Experiment results. In *International Test Conference*, pages 663–672, 1995.

[24] Peter C. Maxwell, Robert C. Aitken, Vic Johansen and Inshen Chiang. The effectiveness of I_{DDQ}, Functional and Scan Tests: How many fault coverages do we need? In *International Test Conference*, pages 168-177, 1992.

[25] Christopher L. Henderson, Jerry M. Soden and Charles F. Hawkins. The behavior and testing implications of CMOS IC logic gate open circuits. In *International Test Conference*, pages 302-310, 1991

[26] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. Digital IC device testing by transient signal analysis (TSA). *Electronics Letters*, 31(18):1568–1570, August 1995.

[27] James F. Plusquellic, Donald M. Chiarulli, and Steven P. Levitan. Simulation experiments investigating digital IC transient response changes in defective and defect-free devices. *Technical Report TR-9612*, Department of Computer Science, University of Pittsburgh, July, 1996.

[28] F. Brglez and H. Fujiwara. A neutral netlist of 10 combinational benchmark circuits and a target translator in FORTRAN. *Special Session on ATPG and Fault Simulation, Int. Symposium on Circuits and Systems*, pages 663-698, June 1985.