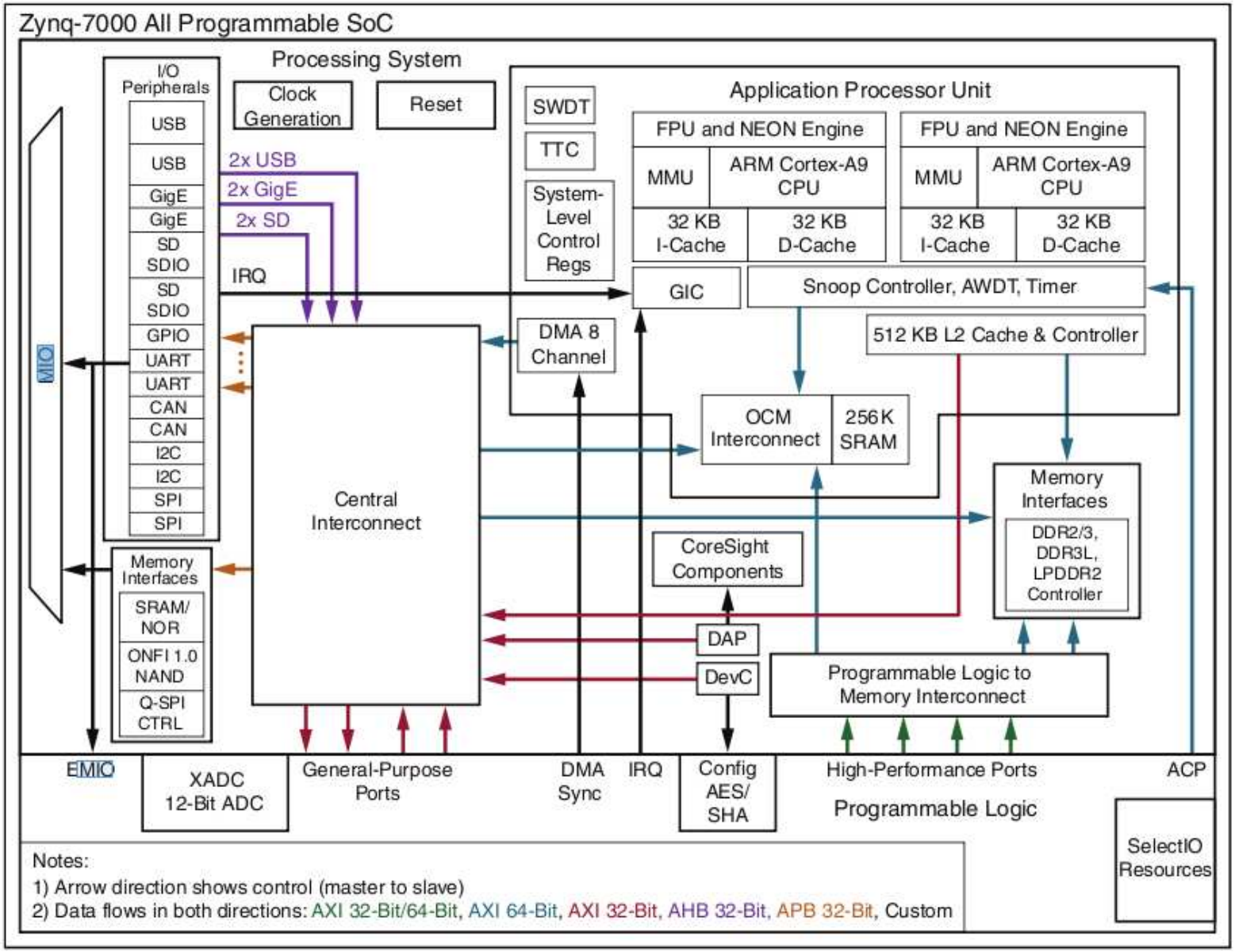
Reference: ZynQ_OVERVIEW_ds190-Zynq-7000-Overview.pdf



MIO and EMIO connection diagram

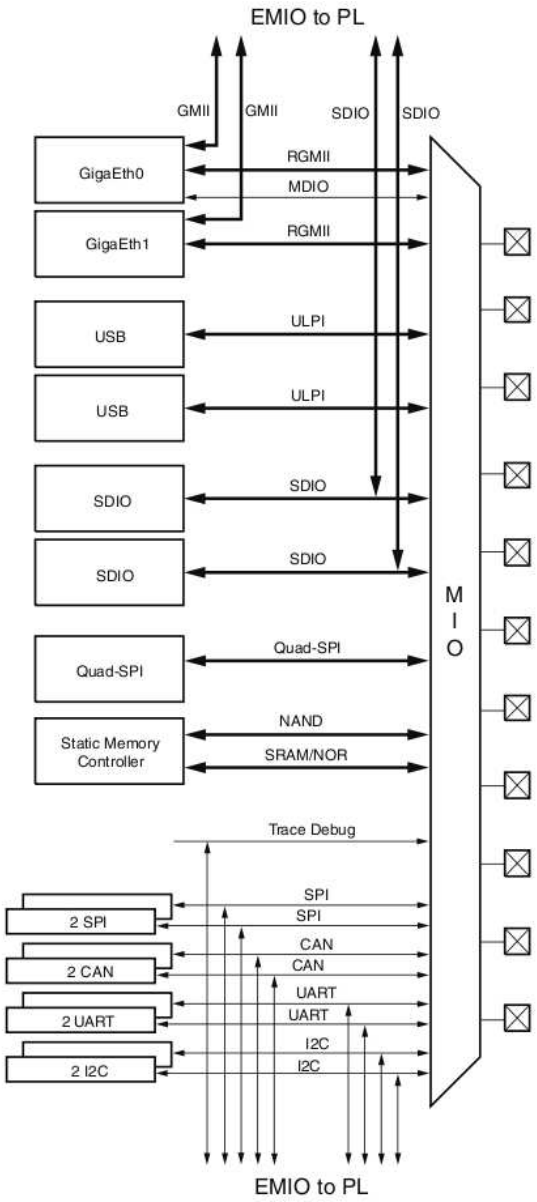


Table 4: **MIO Peripheral Interface Mapping**

Peripheral Interface	MIO	EMIO
Quad-SPI NOR/SRAM NAND	Yes	No
USB 0,1	Yes — External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 54 bits	Yes CAN: External PHY GPIO: Up to 64 bits
GigE: 0,1	RGMII v2.0 External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (Tx and Rx)	Full UART (Tx, Rx, DTR, DCD, DSR, RI, RTS and CTS) either require: Two Processing System pins (Rx and Tx) through MIO and six additional Programmable Logic pins, *or* Eight Programmable Logic pins
Debug Trace Ports	Yes — Up to 16 trace bits	Yes — Up to 32 trace bits
Processor JTAG	Yes	Yes

High Performance AXI ports

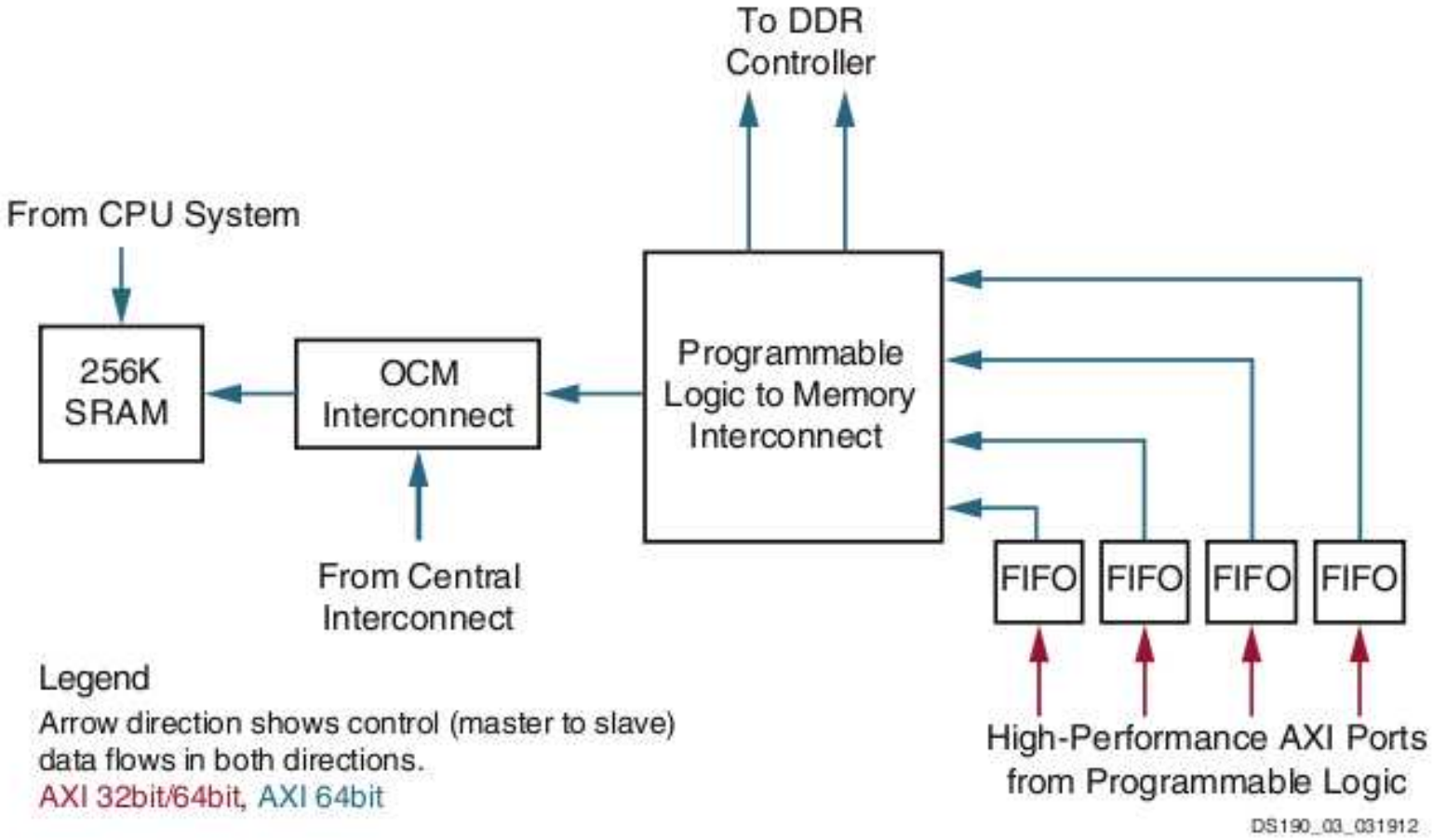


Figure 3: **PL Interface to PS Memory Subsystem**

Zedbard Block Diagram

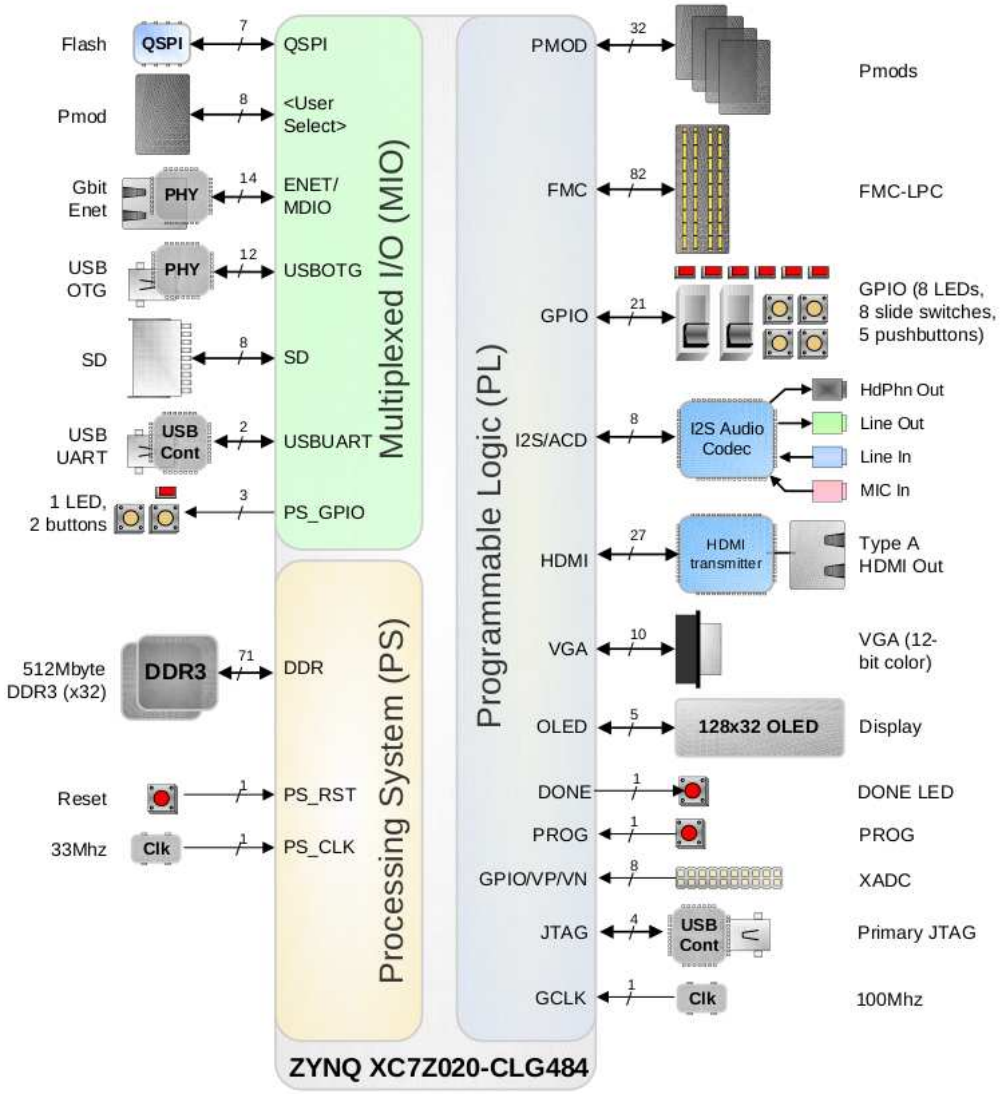


Figure 1 – ZedBoard Block Diagram

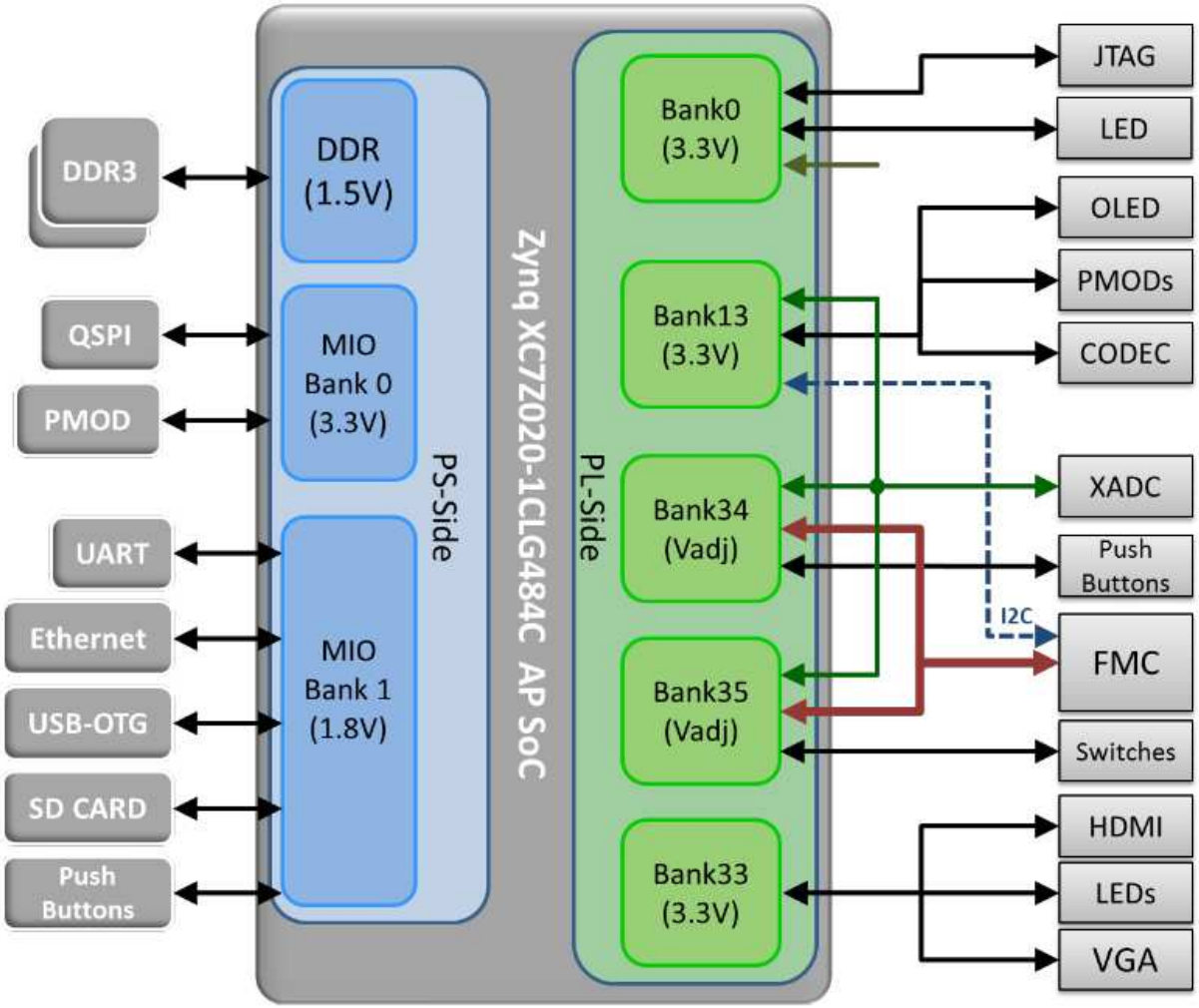


Figure 2 - Zynq Z7020 CLG484 Bank Assignments