LAB Assignment #0, for ECE 338

Assigned Sept. 6th
Due Sept. 13th

Description: Implement and demo a PL-side version of the even detector with switches and leds as input and output

Use the Vivado instruction screencasts to install Vivado, create a project, synthesize a design, generate a bitstream and program the FPGA. Implement a even detector in your VHDL code using the following entity declaration

```
library ieee;
use ieee.std_logic_1164.all;

entity even_detector is
   port(
      a: in std_logic_vector(2 downto 0);
      even: out std_logic
      );
   end even_detector;

architecture arch of even_detector is
   signal p1, p2, p3, p4: std_logic;

   begin

   even <= (p1 OR p2) OR (p3 OR p4);
   p1 <= (not a(2)) AND (not a(1)) AND (not a(0));
   p2 <= (not a(2)) AND a(1) AND a(0);
   p3 <= a(2) AND (not a(1)) AND a(0);
   p4 <= a(2) AND a(1) AND (not a(0));

end arch;
```

This lab is worth 10 points and only involves a hardware demo.

NOTE: ALL ASSIGNMENTS MUST BE PRINTED AND DELIVERED TO THE INSTRUCTOR AT THE BEGINNING OF THE CLASS.