LAB Assignment #2, for ECE 338

Assigned Sept 18th
Due Sept Sept 25th

Description: Create a project with behavioral VHDL and evaluate the behavioral-to-hardware translation process.

Part A: Use Vivado to create a project. Add the following VHDL code which uses an 'indexed' simple assignment within a process block. Open 'elaborated design' and identify components of the schematic that correspond to elements of the VHDL code. Please include your name and the title "Lab #2: Behavioral-to-Schematic Translation, Index Statement".

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity Index is
   Port (
      ctrl: in std_logic_vector(1 downto 0);
      a: out std_logic_vector(3 downto 0)
   );
end Index;

architecture rtl of Index is

signal au: unsigned(3 downto 0);
begin

   process (au, ctrl)
      begin
      au <= (others=>'0');

      au(to_integer(unsigned(ctrl))) <= '1';

      a <= std_logic_vector(au);

      end process;

end rtl;
```

Part B: Use Vivado to create a project. Write your own VHDL code which uses a selected signal assignment and a conditional signal assignment statement to implement two simple functions (your choice), one for each statement, where the entity outputs are a function of the entity inputs (remember, if you do NOT connect your VHDL statement inputs and outputs to the entity inputs and outputs, Vivado will simply delete the statements you write). You are allowed to change the entity inputs and outputs names, size and directions to anything you like, i.e., they do NOT need

to use those given in the VHDL of part A above. But you are not permitted to copy VHDL from any other assignments or from other publicly available sources. Open ‘elaborated design’ and identify components of the schematic that correspond to elements of the VHDL code. Please title “Lab #2: Behavioral-to-Schematic Translation, Selected and Conditional Signal Statements”.

This lab is worth 20 points.