ECE 338: Intermediate Logic Design

Course ID: ECE 338/ECE 595 Intermediate Logic Design

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http://ece-research.unm.edu/jimp
Face-to-face but with Canvas email and discussion board

Department Information

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Course Description

This course provides an introduction to the VHDL hardware description language (HDL) used in the design of electronic systems. Students will learn how to describe a dedicated hardware system using behavioral level VHDL, which will consist of a set of finite state machines. Students will purchase a system-on-chip FPGA and work with Xilinx FPGA computer-aided design (CAD) tools to describe, synthesize, implement and test designs on their FPGA. The Xilinx Zynq FPGA includes both a processor side (PS) and programmable logic (PL) side. The goal of the course is to enable students to translate any type of algorithm written in a programming language, e.g., a C program, into an equivalent set of PL state machines. The state machine representation is more energy efficient and can be designed to leverage parallelism to carry out the tasks associated with the algorithm more quickly. Although the course focuses on describing designs that synthesize to the PL side, advanced topics related to creating designs that enable the integrated on-chip processor to communicate directly to the PL side will be covered.

Course Goals

The goal of this course is to enable you to translate a C program into a behavioral VHDL description that executes as a dedicated hardware engine in the programmable logic of an FPGA. In order to be effective, you will need to be able to translate between C code and VHDL and have knowledge of state-of-the-art commercial FPGA CAD tools.

NOTE This is a laboratory/project based course. Most of your learning will take place as you complete the laboratory and project assignments. The lecture material is supplemental to your learning, i.e., you should become familiar with the tools and techniques described in the lecture material, assimilate and apply those techniques as needed to complete the laboratory and project

assignments. Students in the course will be expected to be able to evaluate the problems, decide on which tools/techniques are relevant and useful for the task, and then adapt and apply them to derive a solution.

Course Objectives/Learning Outcomes

- **C1 (C-to-VHDL):** Demonstrate the ability to translate between C code and VHDL by solving meaningful, real-world problems that executes as a dedicated hardware engine in the programmable logic of an FPGA.
- **C2 (CAD Tools):** Synthesize, implement and test your solution on a FPGA SoC architecture.

Technical Goals

- An important component of Computer Engineering is becoming fluent with Computer-Aided Design tools, such as Xilinx Vivado and Cadence Virtuoso. This course will introduce you to Vivado, which will be used in combination with the C programming language.
- The Computer Engineering discipline is focused on the design and implementation of systems which have hardware components. A key skill to designing such systems is being able to translate between C programs and VHDL. This course will provide guidance and hands-on exercises to give students experience in carrying out C to behavioral VHDL activities using a FPGA as a base platform.

Technical Skills

In order to participate and succeed in this class, you will need to be able to perform the following basic technical tasks:

- Use UNM Canvas.
- Use email, including attaching files, opening files, downloading attachments and open a hyperlink.
- Use a word processor to create homework, laboratory and project reports. NOTE: YOU MUST ONLY SUBMIT TXT and/or PDF files. **WORD, EXCEL or other types of word processing formats will NOT be accepted.**
- Create and upload PDF files.
- Work within a Linux operating system environment, e.g., have knowledge of basic commands including file and directory operations, of software for editing files, of networking concepts, e.g., setting static IPs, configuring routers, etc.
- Have experience with writing, compiling and debugging C programs.
- Have experience with hardware system design concepts, e.g., logic gates, state machines with data paths, etc.
- Install and use computer-aided design (CAD) tools and be familiar with the concepts of logic synthesis, place and route, simulation and timing closure.
- Connect, configure and carry out hardware demonstrations on FPGAs, e.g., powering up an FPGA board, connecting ethernet and USB cables to computers and routers, running serial and network communication and file transfer programs.

Supplemental documentation is provided for computer management tasks

Course Requirements

Students are expected to attend class and actively participate in discussions. Viewing the lecture and lab videos is a mandatory activity, and is supplemental to the face-to-face lectures. In class

quizzes, or quizzes administrated through UNM Canvas, will be given to determine if this requirement is being met. The videos will be extremely useful for improving your VHDL writing skills. Note: 10% of your grade is based on class attendance, participation in class and the quizzes. The course also includes a set of laboratories, a project assignment and (optionally, pending overall class performance) one mid-term exam. There is no final exam, instead students are expected to complete a final project and perform a hardware demonstration.

Technical Requirements

Computer

- A high speed internet connection is highly recommended.
- The main course website is http://www.ece.unm.edu/jimp/vhdl_fpgas
- Any computer capable of running a recently updated web browser should be sufficient to access your online course. However, bear in mind that processor speed, amount of RAM and Internet connection speed can greatly affect performance. Many locations offer free high-speed internet access including UNM's Computer Pods.
- Microsoft Office products are available free for all UNM students (more information on the UNM IT Software Distribution and Downloads page: http://it.unm.edu/software/index.html)

For UNM Canvas Technical Support: (505) 277-0857 (24/7) or use the "Create a Support Ticket" link in your course.

Textbook and Supplemental Materials

Optional Text:

RTL Hardware Design Using VHDL: Coding for Efficiency, Portability, and Scalability, Pong P. Chu, ISBN-13: 978-0-471-72092-8 ISBN-10: 0-471-72092-5

Optional supplementary text:

FPGA Prototyping By VHDL Examples, Xilinx Spartan-3 Version, Pong P. Chu, ISBN: 978-0-470-18531-5

Required Supplementary Materials

- Students will be required to setup an account with Xilinx (www.xilinx.com) as a mechanism to download the Vivado software tool. A free license will be provided by Xilinx.
- Students will be required to buy an FPGA board (at an academic discount price) as covered in the laboratory introductory video(s).

Coursework and Deadlines

Weekly Schedule

- Each module will be covered in 1 week, e.g., Module 1 in week 1, etc.
- Quizzes, when assigned, corresponding to a module MUST be completed in order, and by Sunday at 11pm on the week that the lecture material is covered.
- Laboratory reports and the project report must be submitted on the day that they are due in class.

Every effort will be made to answer student questions within 2 days. NOTE: questions MUST be submitted through UNM Canvas in the discussion forums, and NOT through UNM Canvas email or a personal email to the instructor. You can use email only if I have not responded to a question in 2 days, OR if another student has not provided a satisfactory solution. Students are encouraged

to monitor the discussion board and provide answers to other student questions. I will monitor the questions and chime in as needed. I will make every effort to report grading to students within 1 week of the submission deadline.

Class Effort and Expectations

Please plan on devoting approx. 10 hour per week to cover the lecture material and to do the homework, laboratories and project:

- Students are expected to use the Canvas course email as opposed to a personal email address.
- Students are expected to actively participate in the Canvas discussion board for Q&A.
- Students are expected to communicate with one another on laboratory and project assignments, but you are not permitted to share VHDL code or other written components of assignments or the project.
- Students are expected to keep abreast of course announcements.
- Students are expected to keep instructor informed of class related problems, or problems that may prevent the student from full participation.
- Students are expected to address technical problems immediately.
- Students are expected to observe course netiquette at all times.

Grading Procedures

All laboratories and the project are designed to be tied directly to the core material in this course. Becoming efficient at behavioral VHDL requires hands-on experience, i.e., lecture material is important but most of your learning will occur while designing solutions, testing them through simulation and hardware experiments, and examining how the tools synthesize designs to implementations. Therefore, a large portion of the grade is allocated to labs and projects, as shown below.

Grading Policy

I will accept late work but please submit your initial attempt by the indicated times. Late work will be automatically be assigned half-credit if submitted after the deadline, so turn in whatever you can before the deadline. Also, all the work in this class is cumulative so if you fall behind, it will be very hard for you to catch up.

If you anticipate difficulty in meeting a deadline, you need to notify me at least 1 day in advance of the deadline and be prepared to provide evidence explaining why you will be late.

All written work needs to be printed out and submitted in class.

Grading Distribution and Description

The distribution of weights for the exams, laboratories and projects is as follows:

Midterm	30%
Laboratories	30%
Project	30%
Participation (5%) and Quizzes (5%)	10%

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Midterm Exam: The mid-term exam is optional. If the class performs well on the laboratories and project milestones, I will NOT give a midterm exam, and instead, I will reallocate the 30% evenly to laboratories and the project (both will become 45% of your grade). If the midterm is given, it will consist entirely of short answer types of questions. A sample exam is provided to enable students to be prepared for the type of questions they will be expected to answer. Your written answers will be assessed according to the level of understanding that you have of the subject matter, i.e., primarily on the correctness of your answer, but also on the conciseness of your answer. Focus on answering the question and avoid writing 'everything you know' about the topic. The exam is designed to give you enough time to write concise answers to the questions.
Laboratories: Students purchase an FPGA board at the beginning of the course and work through a series of laboratories to become familiar with the process of creating programming bitstreams for the FPGA using computer-aided design tools, e.g., Xilinx Vivado. The initial set of laboratories will train you on the use of the Vivado. The remaining laboratories (and project) are designed to give you experience working on an actual problem, e.g., a game project. The laboratory reports are graded according to the rubrics defined below.
Project: Students will work in groups of two to implement a video game. I will provide a default game project that will build on the example 'pong' game covered in the lecture slides, but students are encouraged to find a game that they will enjoy working on. No parts of the game can be provided on public websites for download. Game development MUST be done entirely by the two students in each group. A project hardware demonstration and a project report are due at the end of the term to assess the student's mastery of VHDL. The project report is graded according to the rubrics defined below.
Discussions: Students are expected to participate actively in Canvas discussion boards by asking and answering questions that other students or the instructor posts. Participation on discussion boards represents at least half of the 'Participation' component of your grade. At least one post which asks a question, provides a comment or an answer to another student's question is required from each student in half of the modules in order to receive full credit for participation. Student engagement will be monitored by the instructor and exceptional interaction will be rewarded with extra credit.
Participation: Enrollment will be taken at the beginning of each class. Students missing more than 2 classes will be assessed a penalty on the 'Participation' component of their grade. Class and discussion board participation is used by the instructor to determine which (if any) students are having difficulty, and to identify those students who are exceptional.
Summary of Course Work: There are a series of laboratories each of which is considered an 'Assignment' and requires a laboratory report. You are also expected to participate in class and in at least half of the discussion forums associated with each of the modules. An optional mid-term and the final project are also components of the required work in this course.

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

Cheating at any time in this course will cause you to fail the course.
For a complete description of academic dishonesty, refer to the UNM Student Handbook.

<u>Laboratory and Project Rubrics</u>

- 20% Description
  Does the report minimally include the following components: title, introduction to the lab that

describes the problem to be solved, a body section that shows how the problem was solved (with schematic and supporting waveforms, if needed), and concluding remarks on the results and the student's experience?

- 20% Correctness
  Is the problem solved correctly?
- 20% Completeness
  Are all the steps needed to solve the problem explicitly shown. For example, are the schematic diagram and the boolean equations given? Is the code given? Are the waveforms given? Are there comments in the Verilog code? Depending on the requirements given in the lab description, some of these components are not needed.
- 20% Clarity/Conciseness
  Are the description and results clearly and concisely presented or is there unnecessary clutter or redundancy?
- 20% Quality of write-up
  Is the lab report easy to read? Are the figures, plots, etc. neatly and professionally presented, i.e., in electronic form with arrows and text explaining the important features? Is the information on the title page complete, with a meaningful title and the student's name.

Grading Scale

A+	(97-100)
A	(93-96)
A-	(90-92)
B+	(87-89)
B	(83-86)
B-	(80-82)
C+	(77-79)
C	(73-76)
C-	(70-72)
D+	(67-69)
D	(63-66)
D-	(60-62)
F	(0-59)

Netiquette

- In following with the UNM Student Handbook, all students will show respect to their fellow students and instructor when interacting in this course. Take Netiquette suggestions seriously. Flaming is considered a serious violation and will be dealt with promptly. Postings that do not reflect respect will be taken down immediately.
- This course encourages different perspectives related to such factors as gender, race, nationality, ethnicity, sexual orientation, religion, and other relevant cultural identities. The course seeks to foster understanding and inclusiveness related to such diverse perspectives and ways of communicating.

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UNM Policies

Title IX: Gender Discrimination

In an effort to meet obligations under Title IX, UNM faculty, Teaching Assistants, and Graduate Assistants are considered "responsible employees" by the Department of Education (see page 15 - http://www2.ed.gov/about/offices/list/ocr/docs/qa-201404-title-ix.pdf). This designation requires that any report of gender discrimination which includes sexual harassment, sexual misconduct and sexual violence made to a faculty member, TA, or GA must be reported to the Title IX Coordinator at the Office of Equal Opportunity (oeo.unm.edu). For more information on the campus policy regarding sexual misconduct, see: https://policy.unm.edu/university-policies/2000/2740.html

Copyright Issues

All materials in this course fall under copyright laws and should not be downloaded, distributed, or used by students for any purpose outside this course.

Accessibility

The American with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodations of their disabilities. If you have a disability requiring accommodation, please contact the UNM Accessibility Resource Center in 2021 Mesa Vista Hall at 277-3506 or http://as2.unm.edu/index.html. Information about your disability is confidential.

- Blackboard's Accessibility statement: http://www.blackboard.com/accessibility.aspx

Academic Misconduct

You should be familiar with UNM's Policy on Academic Dishonesty and the Student Code of Conduct (http://pathfinder.unm.edu/code-of-conduct.html) which outline academic misconduct defined as plagiarism, cheating, fabrication, or facilitating any such act.

Drop Policy

UNM Policies: This course falls under all UNM policies for last day to drop courses, etc. Please see http://www.unm.edu/studentinfo.html or the UNM Course Catalog for information on UNM services and policies. Please see the UNM academic calendar for course dates, the last day to drop courses without penalty, and for financial disenrollment dates.

UNM Resources

CAPS Tutoring Services http://caps.unm.edu/programs/online-tutoring/

CAPS is a free-of-charge educational assistance program available to UNM students enrolled in classes. Online services include the Online Writing Lab, Chatting with or asking a question of a Tutor.

Embedded Tutor - if this course has a tutor assigned, substitute the following:

This course has tutoring services incorporated into the course. Please see the "CAPS Tutor" link in the course menu on the left for more details.

UNM Libraries http://library.unm.edu

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Student Health & Counseling (SHAC) Online Services

Schedule of Activities
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Date	Lecture
Week 1	Introduction
Week 2	Overview of VHDL
Week 3	Overview of VHDL
Week 4	Concurrent Signal Assignment Stmts
Week 5	Concurrent Signal Assignment Stmts
Week 6	Sequential Statements in VHDL
Week 7	Sequential Statements in VHDL
Week 8	fall break
Week 9	Finite State Machines
Week 10	Finite State Machines
Week 11	Register Transfer Methodology
Week 12	Register Transfer Methodology
Week 13	Register Transfer Methodology
Week 14	Thanksgiving
Week 15	Register Transfer Methodology
Week 16	Project Demos
	Final exam

(Note: Changes/Additions to this schedule will be posted on my web site http://www.ece.unm.edu/jimp/vhdl_fpgas and on UNM Canvas)