

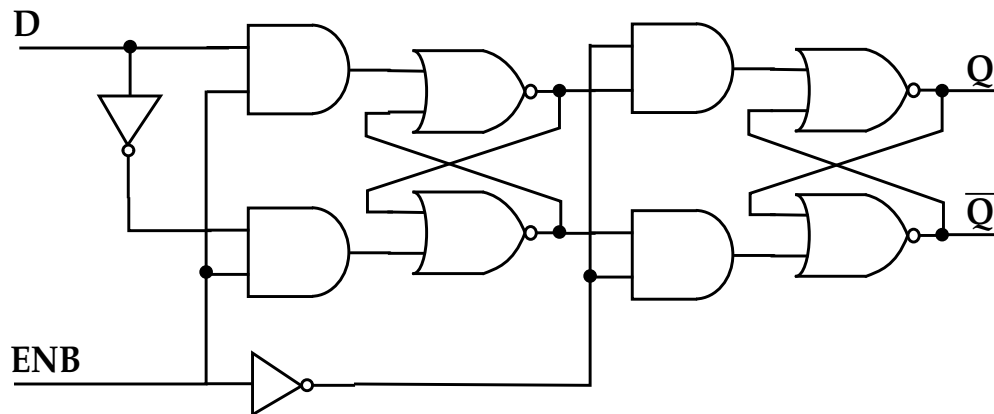
## LAB Assignment #4 for CMPE 413/CMSC 711

Assigned: Friday, Sept 29th

Due: Friday, Oct 13th

**Description: Layout and simulate (using Virtuoso and Spectra) both a transmission-gate master-slave flip-flop and a gate-level version:**

- Layout the transmission gate flip-flop discussed in class (Basics slide set).
- Layout the gate-level version shown below:



### Report Requirements:

- 1) Print out the layouts.
- 2) Run tests and generate plots to show that both flip-flops work correctly.
- 2) For ONLY one of the flip-flops (your choice), determine the maximum clock frequency (minimum clock period) and the maximum clock skew (maximum variation in the time between a transition of Clk and the corresponding transition of Clk\_bar that preserves correct operation of the flip-flop). Note, you will have to remove the inverter and drive Clk and Clk\_bar using input statements for the clock skew experiments.

For example, pick some realistic rise and fall times for your source statements (input signals) in Spectra and use them for all of your tests, e.g., 250ps to 1ns.

Show me a plot of D, Q, Q\_bar, Clk and Clk\_bar of the flip-flop working correctly.

### Maximum Clock Frequency:

Report the maximum clock frequency of the flip-flop. Determine this time for both possible values of D (logic 0 and 1) with opposite initial values stored in the flip-flop. Show me plots of the flip-flop working and not working.

### Clock Skew Experiments:

Report the maximum amount of clock skew for two cases:

- When Clk\_bar changes before Clk.
- When Clk\_bar changes after Clk.

This value will be different when:

- D is high and the flip-flop stores a zero.
- D is low and the flip-flop stores a high value.

Show me plots of the flip-flop working and not working under each case.

Choose a clock frequency that allows your flip-flop to work correctly. This frequency will be something slightly less than the maximum clock frequency you found above. For example, if you determined that your flip-flop can switch at 120MHz (about 9ns), then choose 110MHz to evaluate it for clock skew.