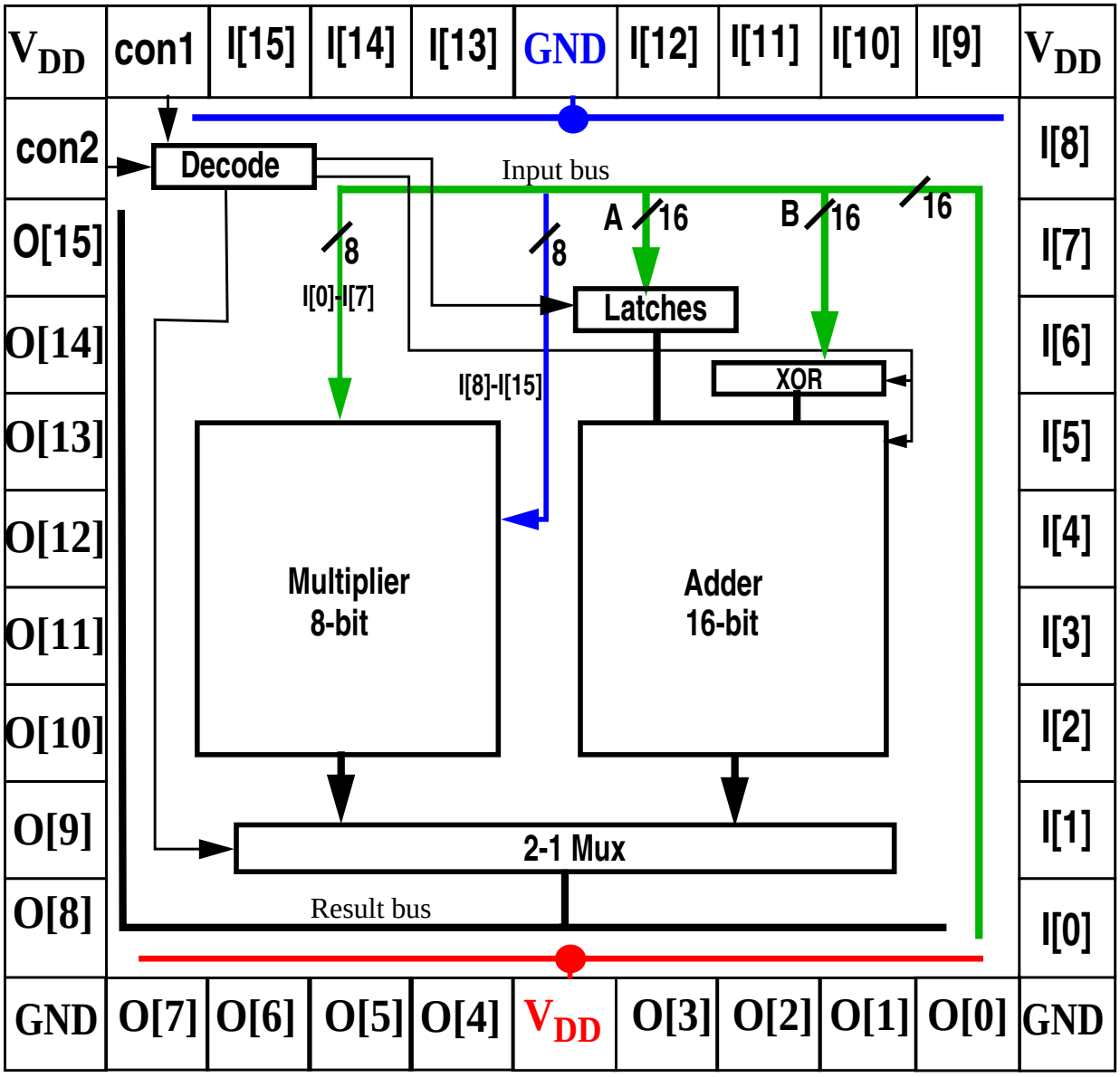
CMPE 413/ CMSC 711

Project Specification: 16 bit 2's complement Adder and 8 bit 2's complement multiplier.

Assigned: Fri, Nov 3rd
Due: Tue, Dec. 19th

Description:



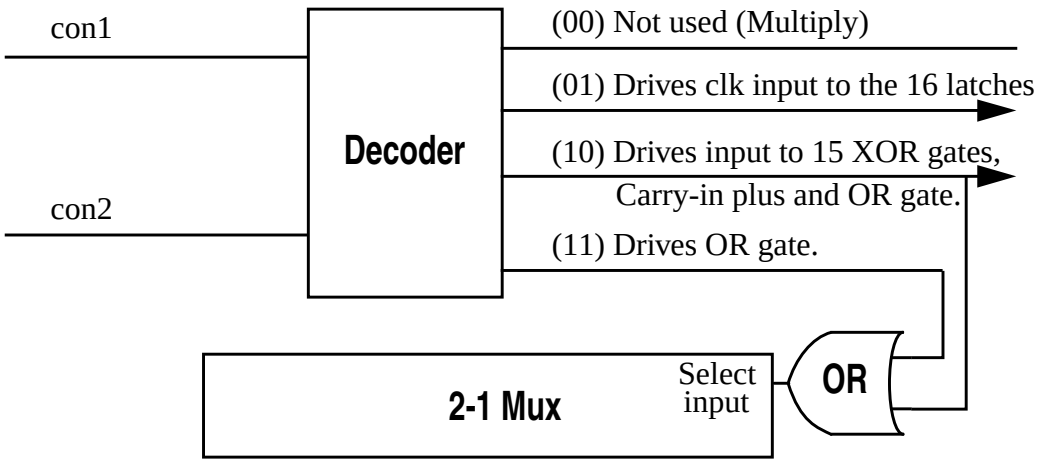
Your assignment is to design, implement and simulate a 2's complement 16-bit combinational ADDER and 8-bit combinational MULTIPLIER circuit. The ADDER will be able to add or subtract using a carry-in control bit. A block diagram as well as the pin-out of the circuit is shown above. YOU MUST USE THIS PADFRAME DEFINITION so we can test the parts after they are fabricated. I'll provide the padframe on my web page.

The Decoder takes 2 inputs and produces the outputs given in the truth table below:

Table 1: Control Table

Con2/ Con1	Function	Description
00	Select MULT	Setting Con2 to 0 selects MULTIPLIER output for result bus.
01	Latch A operand to adder (NOTE: You MUST use a negative edge-triggered FF).	Put A operand on I[15]-I[0], toggle Con1 from 1 to 0 (negative edge-triggered FF), put B operand on I[15]-I[0].
10	Subtraction	Setting Con2 to1 selects ADDER output for result bus (see diagram below).
11	Addition	Setting Con2 to1 selects ADDER output for result bus.

NOTE: You MUST use a negative edge-triggered FF to latch the A operand.
NOTE: The 2-to-1 select MUX must OR the one hot wires for subtraction and addition:



Report Requirements:

1) Describe the project and provide the specifications as given above. Comment on your experience with doing this project (good and bad).
2) Draw block level diagrams of each component of your design, adder, multiplier, latch, mux, etc. Draw a floor plan (block level diagram with data paths) showing how each component is connected to the other ones.
3) Write VHDL code and simulate it for the individual components and for the entire design.
4) Generate a schematic diagram from the VHDL code.

3) Do the layout. Verify the layout against the schematic using LVS. You must provide output from LVS indicating that the match was successful, similar to the requirements of lab 5. Print portions of your layout (the most important parts) and briefly describe them.
4) Simulate the individual components, e.g., MULTIPLIER, ADDER, etc, of the layout using Spectre (extra credit if you've simulated the VHDL, generated schematic and verified using LVS). Turn in CLEARLY labeled plots showing functional operation under several different values of A and B. You will probably not be able to simulate the entire design with the pad frame. Extra credit will be given for simulations of the entire design withOUT the pad frame. Please do NOT simulate the pad frame in Spectra. You will not be allowed to fabricate unless you simulate the ENTIRE design at either the VHDL or Spectra level. Note that if you do it at the VHDL level, you MUST also show that the layout conforms to the VHDL spec using schematic and LVS.

THIS DESCRIPTION and the set of requirements are subject to change. Please monitor the web page for updates.

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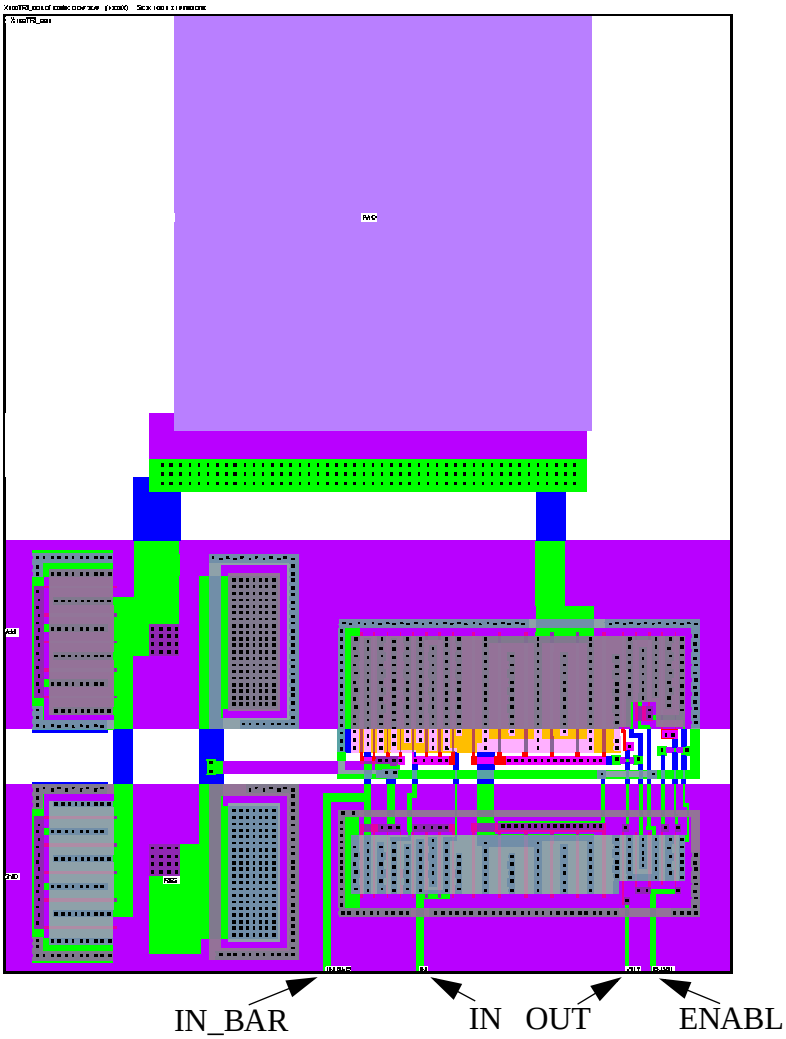
The 0.5um I/O pad layout is shown below:



There are four places to connect wires. At least two connections MUST be made on every I/O pad.

In order to configure the I/O pad as an INPUT pad (get signals from the outside world into the core logic), you MUST tie ‘enable’ to GND. In this case, connect to ‘IN’ and ‘IN_BAR’ to obtain the input signal and its complement, respectively.

In order to configure as an OUTPUT pad, tie ‘enable’ to VDD and drive ‘OUT’ with your signal.

X100TRI_001 (Tri-State I/O Pad)

input:

IN = PAD

IN_BAR = !PAD

output:

PAD = ((ENABL & OUT) | (!ENABL & highz))

The following schematic is for a 2.0um I/O pad (not the 0.5um pad shown above) but the configuration is the same.