Exam II

Name:

1) a) (6pts) Draw and label the three components of load capacitance (C_L) at the output of a CMOS logic gate.

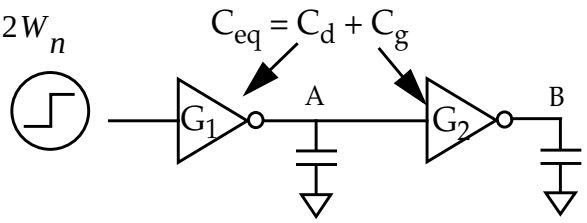
b) (8pts) Briefly explain the characteristics of a self-loaded node.

As a designer in charge of a performance-optimized layout, how can you take advantage of nodes that are dominated by self-loading.

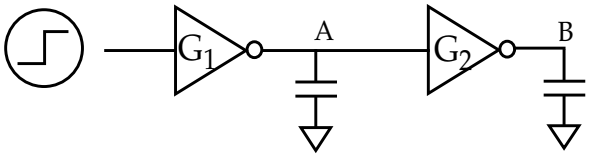
Identify 2 elements of a design, e.g. microprocessor, that are likely to be composed of nodes that are NOT self-loaded.

c) (6pts) Prove, using RC_{eq}, that overall delay is not changed between points A and B in the following 2 circuit configurations. Assume the channel resistance per unit area of p-channel devices is twice that of n-channel devices.:

Assume $W_p = 2W_n$



Assume $W_p = W_n$

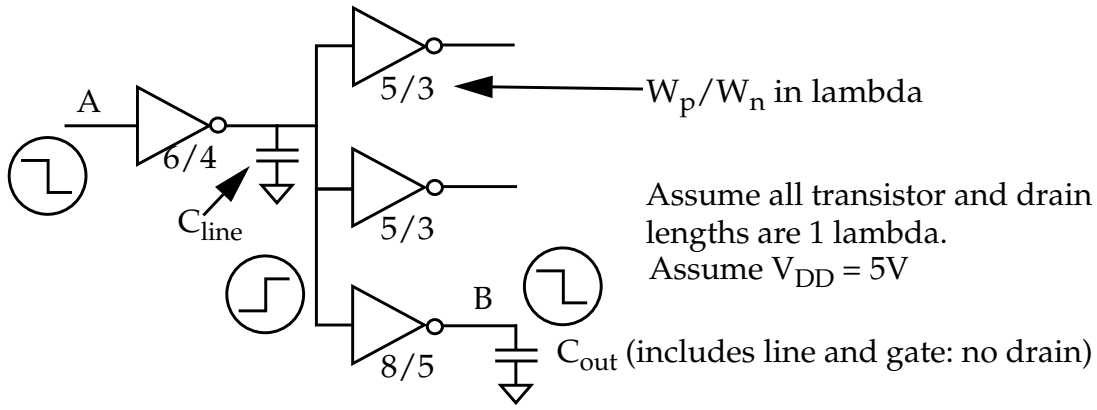


d) (5pts) Briefly explain the sources of variation that require design margining. We discussed design corners in terms of the two environmental sources of variation. Draw the box and label the corners that must be tested through simulation, showing the position of fast and slow transistors that result from the manufacturing source of variation.

2) a) (5pts) Using the simple gate delay model, compute the fall time, t_f, given the following:

$$\beta_n = 100\frac{W}{L}\mu A/V^2 \qquad k = 3 \qquad V_{DD} = 3.3 \qquad C_L = 50\,fF$$

b) (12pts) Estimate the delay between nodes A and B for a **falling** transition on A using the simple gate delay model. SHOW YOUR WORK CLEARLY !



Given: C_{line} = 20 fF and C_{out} = 100fF and k = 4 and

$$\beta_n = 75\frac{W}{L}\frac{\mu A}{V^2} \quad \text{and} \quad \beta_p = 40\frac{W}{L}\frac{\mu A}{V^2}$$

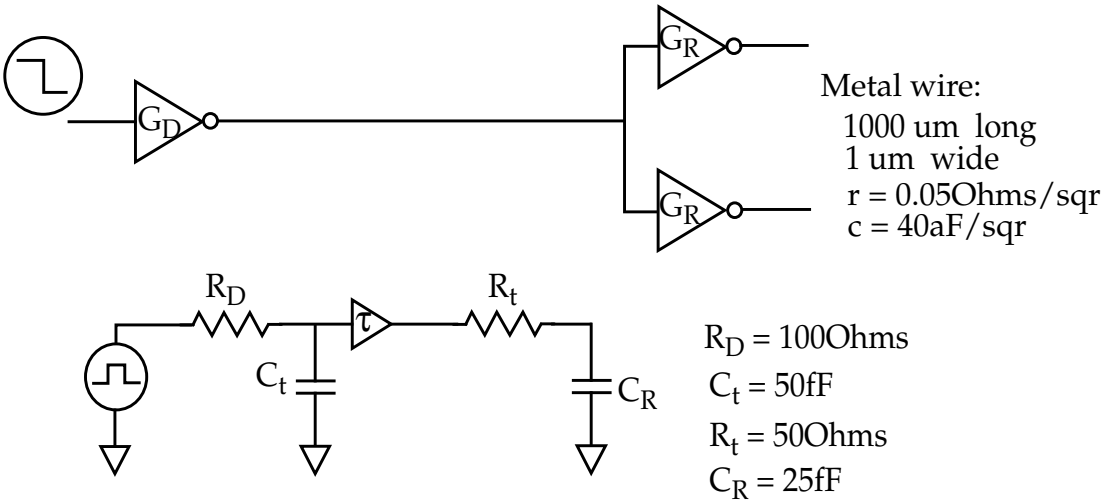
Assume n-trans drain (perimeter + area) and gate capacitance per square lambda are:

$$C_{dn} = 2.0\,fF \quad \text{and} \quad C_{gn} = 2.5\,fF$$

Assume p-trans drain (perimeter + area) and gate capacitance per square lambda are:

$$C_{dp} = 3.0\,fF \quad \text{and} \quad C_{gp} = 4.0\,fF$$

c) (8pts) Estimate the delay from G_D to G_R using the distributed RC model. SHOW YOUR WORK CLEARLY !

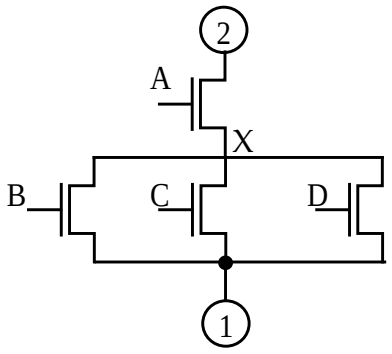


3) a) (6pts) Convert the following expression into the appropriate form for use in a NOR-NOR PLA. Show your work. Draw the NOR gate schematic diagram that results.

$$F_1 = b_1 b_2 \overline{b}_3 \overline{b}_4 + \overline{b}_1 b_2 b_3 \overline{b}_4$$

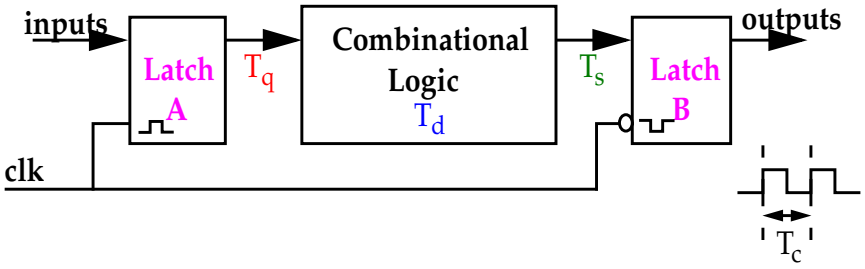
b) (6pts) Using the following n-channel network for function F, indicate the point (1 or 2) to connect to GND in order to yield a gate with the best performance. Assume that the input signal arrival times are **un**known. Briefly explain your choice with reference to the source/drain capacitance at node **1**.

$F = \overline{(B+C+D).A}$



c) (4pts) With reference to your answer in part c, would your choice change if signal A is the first arriving signal? Why or why not? (Hint: Make reference to the source/drain capacitance at node X).

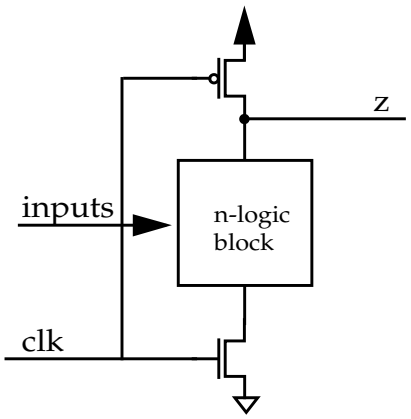
d) (3pts) Define the timing constraint that must be met in order for this circuit to operate properly, in terms of T_C, T_q, T_s, and T_d. Assume that Latch A is positive level-sensitive and Latch B is negative level-sensitive.



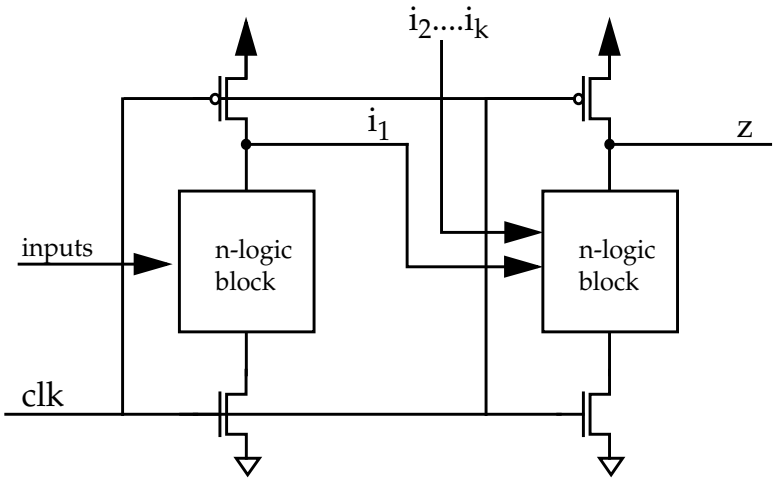
e) (6pts) Briefly explain the two sources of clock skew in a global clock generation strategy.

4) a) (4pts) List the advantage(s) of pseudo-NMOS over full complementary CMOS. List the disadvantage(s).

b) (7pts) Briefly explain the condition necessary for a gate to be considered dynamic. Briefly explain the operation of the following dynamic logic gate, in terms of precharge and evaluate clock phases. List the advantage(s) and disadvantage(s) over full-complementary CMOS.



c) (8pts) Briefly explain how the following dynamic logic cir cuit can fail, using timing diagrams for clk, i_1 and z. How does CMOS domino logic solve this problem?



e) (6pts) In the following circuit, assume that phi_1 and phi_2 are non-overlapping clocks. Briefly explain how this circuit can be used to implement a master-slave flip-flop using a timing diagram with D, phi_1, phi_2 and Q. Modify this gate so that the degraded logic value at nodes A and B is fully restored.