MOS Transistor Definitions

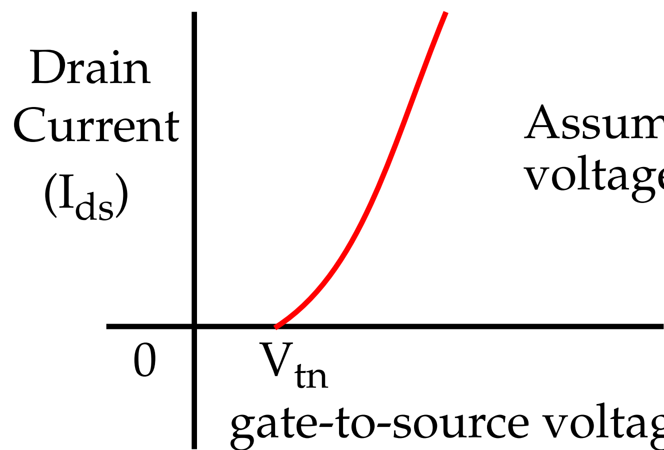
n-type MOS: Majority carriers are electrons.

p-type MOS: Majority carriers are holes.

Positive/negative voltage applied to the gate (with respect to substrate) enhances the number of electrons/holes in the channel and increases conductivity between source and drain.

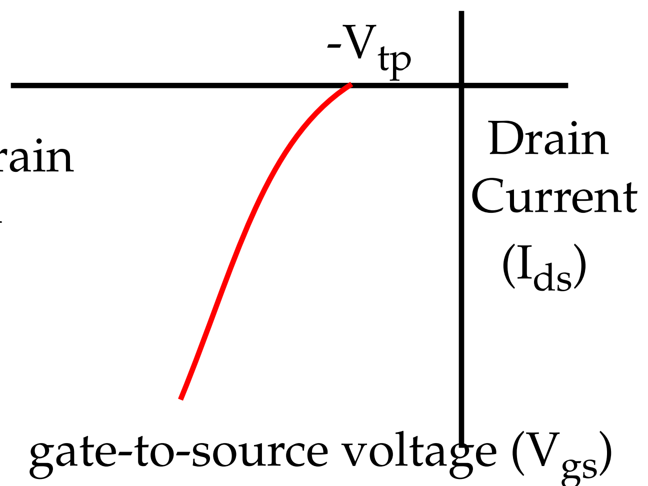
V_t defines the voltage at which a MOS transistor begins to conduct. For voltages less than V_t (threshold voltage), the channel is cut off.

n-channel enhancement MOS



Assume source-to-drain voltage (V_{ds}) is fixed

p-channel enhancement MOS



MOS Transistor Definitions

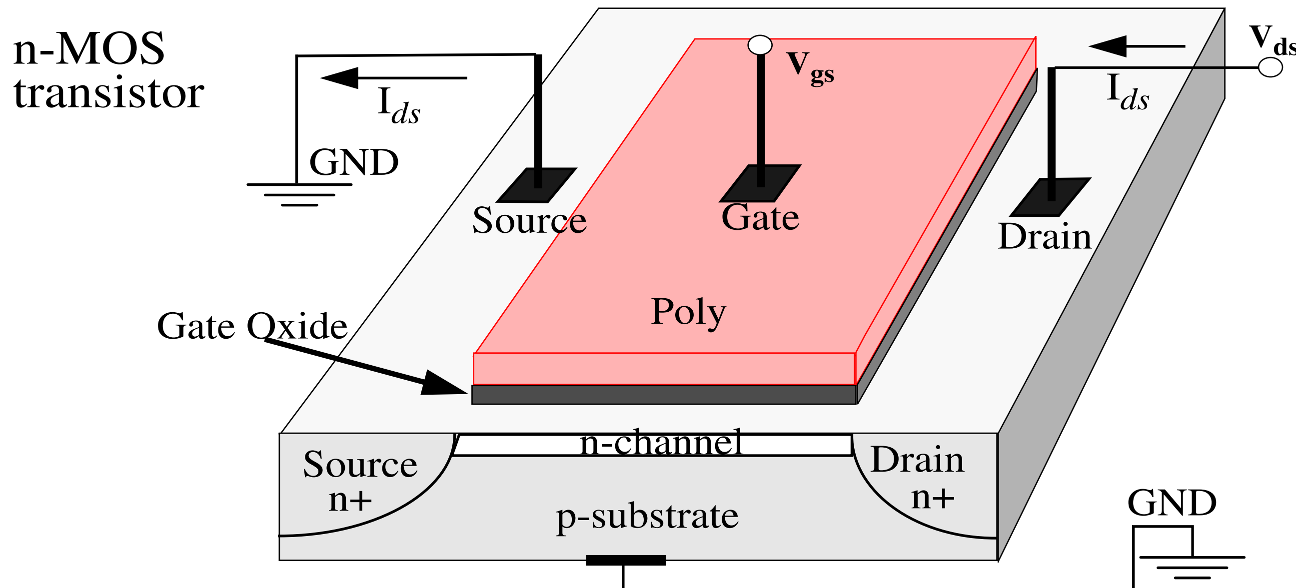
In normal operation, a positive voltage applied between source and drain (V_{ds}).

No current flows between source and drain ($I_{ds} = 0$) with $V_{gs} = 0$ because of back to back pn junctions.

For n-MOS, with $V_{gs} > V_{tn}$, electric field attracts electrons creating channel.

Channel is p-type silicon which is inverted to n-type by the electrons attracted by the electric field.

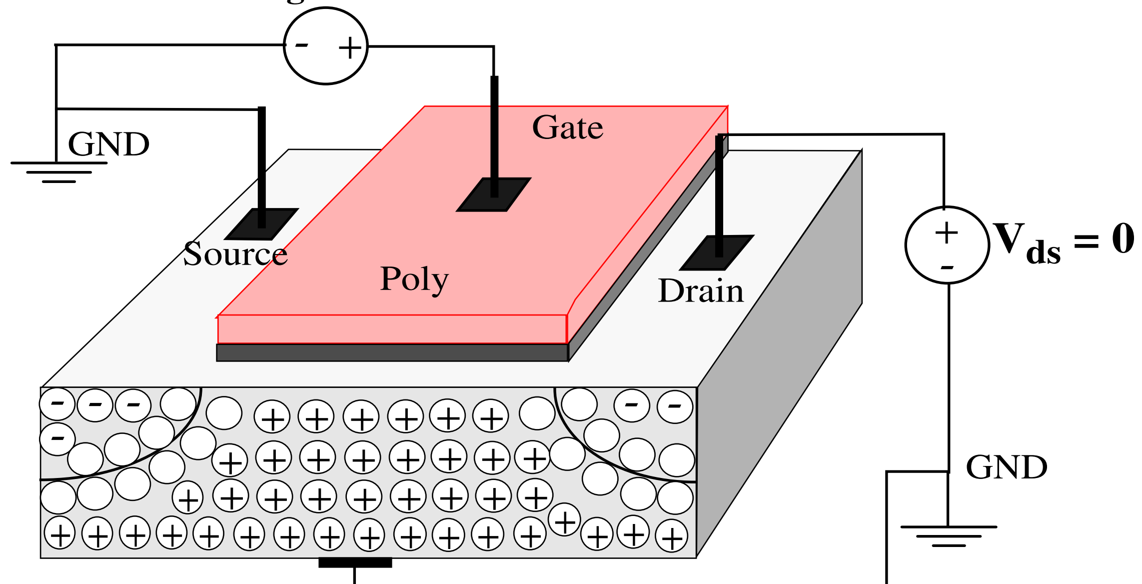
n-MOS
transistor



n-MOS Enhancement Transistor Physics

Three modes based on the magnitude of V_{gs}: accumulation, depletion and inversion.

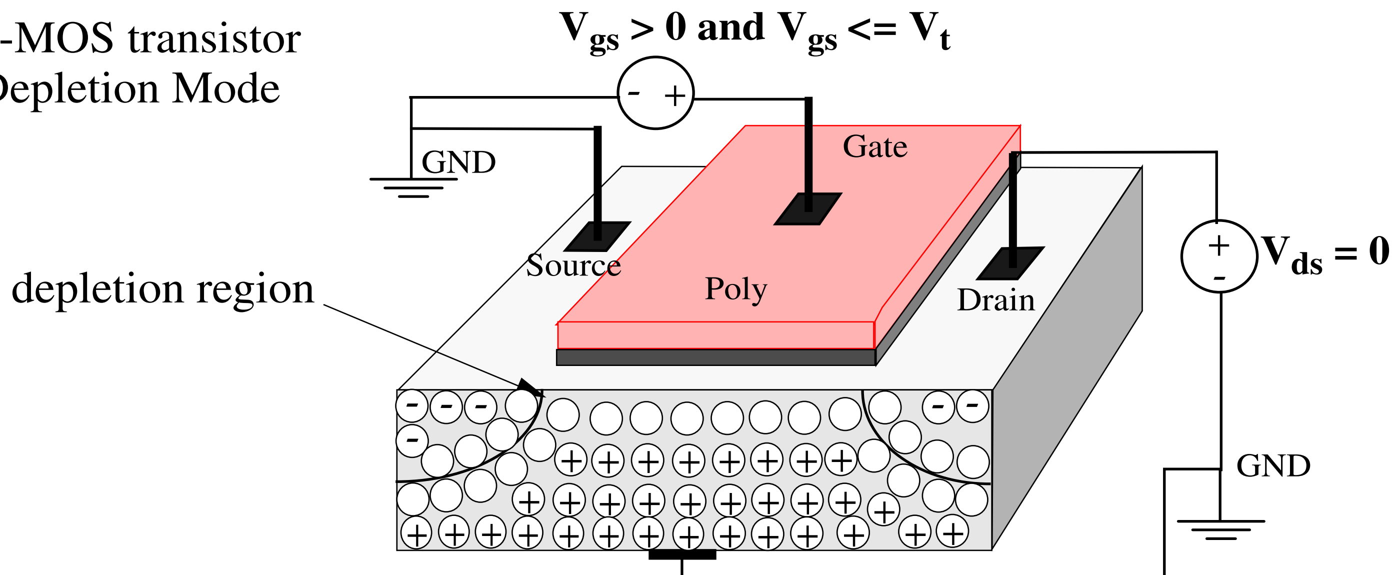
n-MOS transistor
Accumulation Mode



n-MOS Enhancement Transistor Physics

n-MOS transistor
Depletion Mode

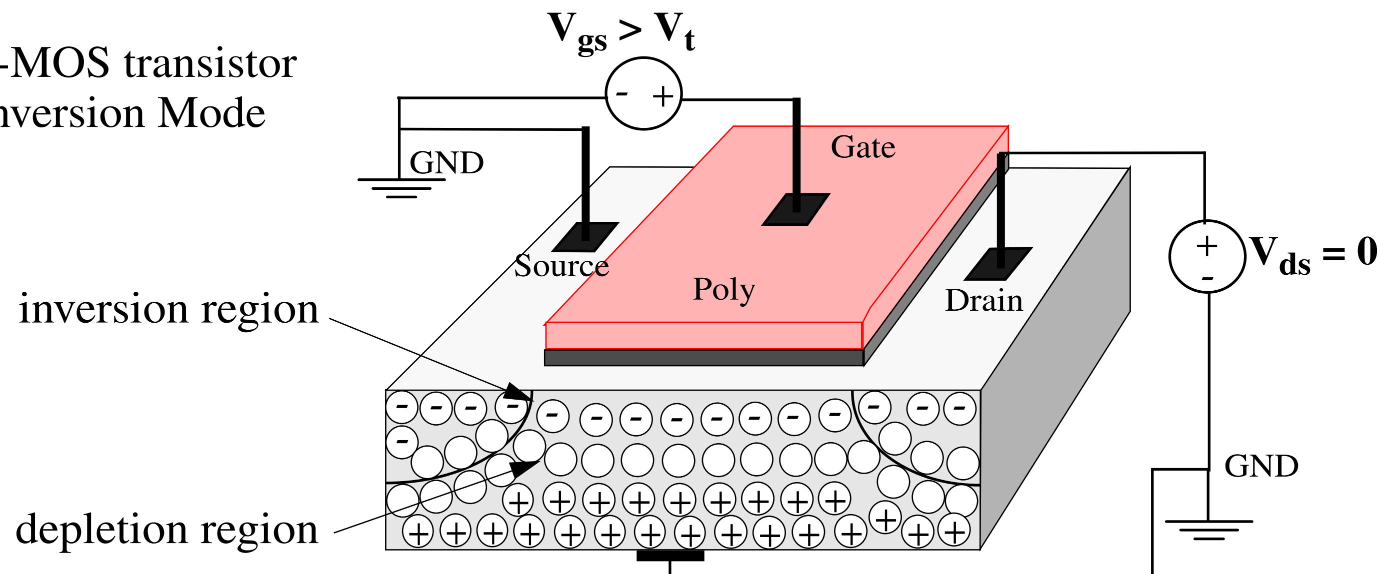
depletion region



n-MOS transistor
Inversion Mode

inversion region

depletion region



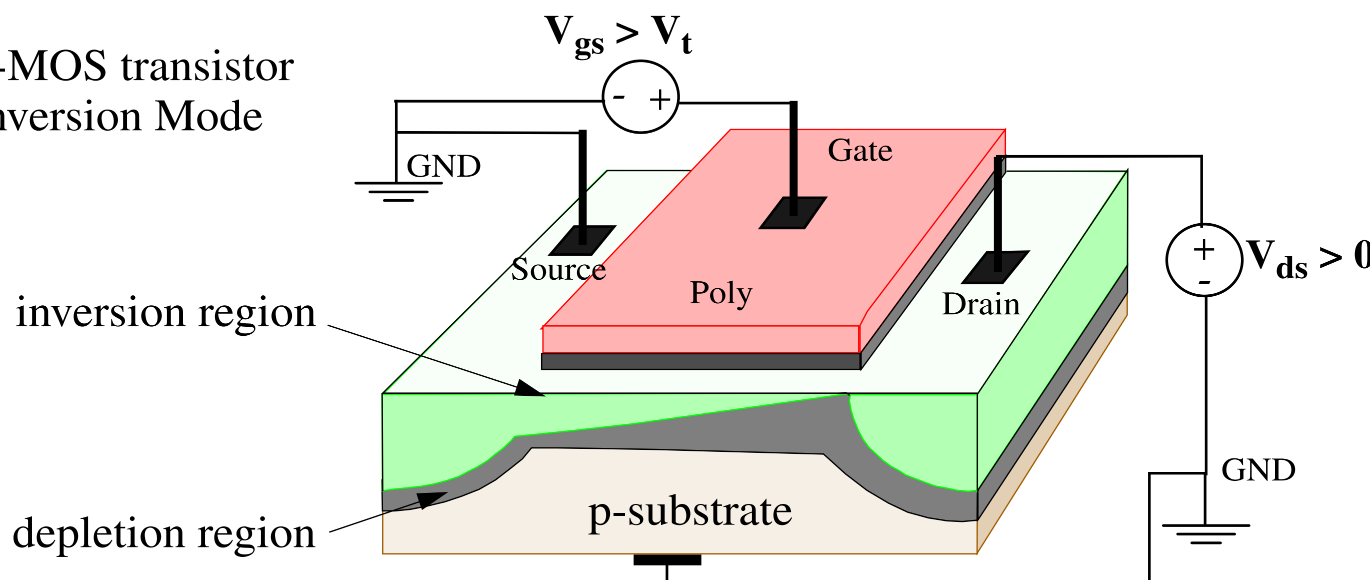
n-MOS Enhancement Transistor

With V_{ds} non-zero, the channel becomes smaller closer to the drain.

When $V_{ds} <= V_{gs} - V_t$ (e.g. $V_{ds} = 3V$, $V_{gs} = 5V$ and $V_t = 1V$), the channel reaches the drain (since $V_{gd} > V_t$).

This is termed **linear**, **resistive** or **nonsaturated** region. I_{ds} is a function of both V_{gs} and V_{ds}.

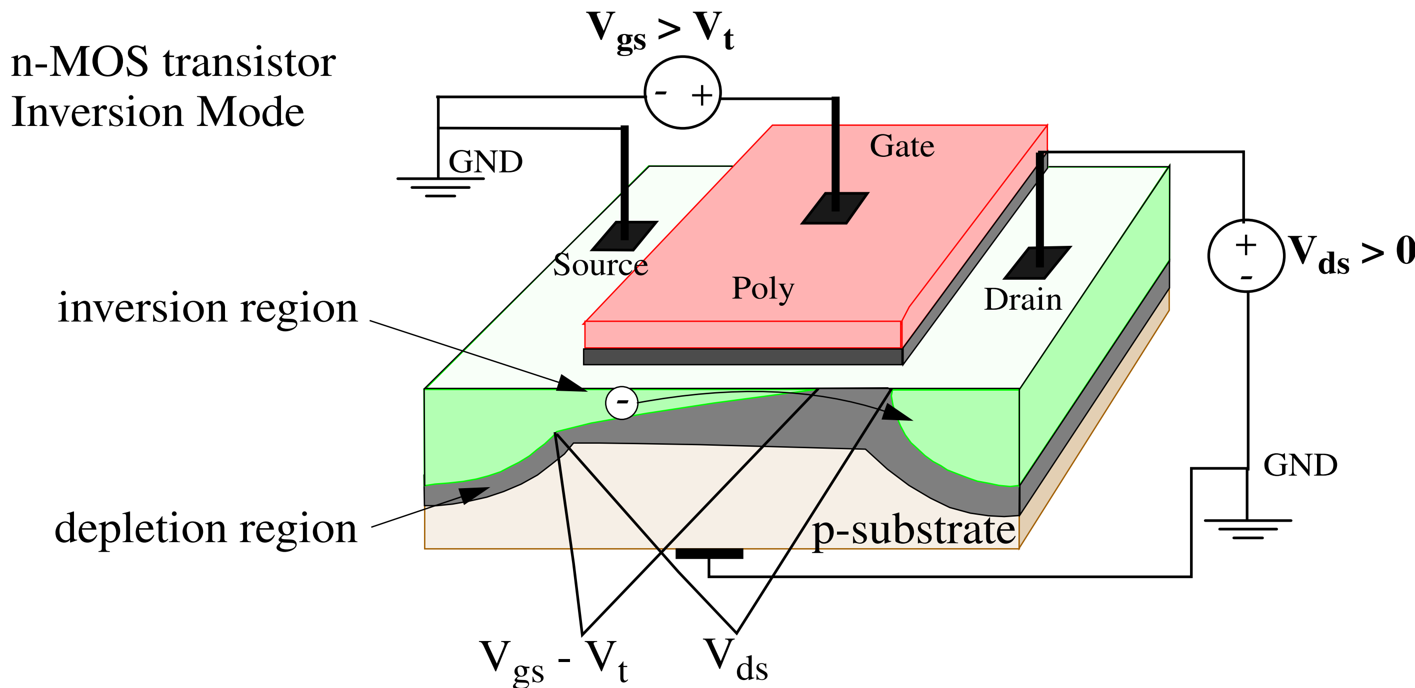
n-MOS transistor
Inversion Mode



n-MOS Enhancement Transistor

When $V_{ds} > V_{gs} - V_t$ (e.g. $V_{ds} = 5V$, $V_{gs} = 5V$ and $V_t = 1V$), the channel is *pinched* off close to the drain (since $V_{gd} < V_t$).

This is termed saturated region. I_{ds} is a function of V_{gs}, almost independent of V_{ds}.



MOS Enhancement Transistor

MOS transistors can be modeled as a voltage controlled switch. I_{ds} is an important parameter that determines the behavior, e.g., the speed of the switch.

What are the parameters that effect the magnitude of I_{ds}? (Assume V_{gs} and V_{ds} are fixed, e.g. 5V).

- The distance between source and drain (channel length).
- The channel width.
- The threshold voltage.
- The thickness of the gate oxide layer.
- The dielectric constant of the gate insulator.
- The carrier (electron or hole) mobility.

Summary of normal conduction characteristics:

- *Cut-off*: accumulation, I_{ds} is essentially zero.
- *Nonsaturated*: weak inversion, I_{ds} dependent on both V_{gs} and V_{ds}.
- *Saturated*: strong inversion, I_{ds} is ideally independent of V_{ds}.

Threshold Voltage

V_t is also an important parameter. What effects its value?

Most are related to the material properties. In other words, V_t is largely determined at the time of fabrication, rather than by circuit conditions, like I_{ds}.

For example, material parameters that effect V_t include:

- The gate conductor material (poly vs. metal).
- The gate insulation material (SiO_2).
- The thickness of the gate material.
- The channel doping concentration.

However, V_t is also dependent on

- V_{sb} (the voltage between source and substrate), which is normally 0 in digital devices.
- Temperature: changes by -2mV/degree C for low substrate doping levels.

Threshold Voltage

The expression for threshold voltage is given as:

$$V_t = 2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_b}}{C_{ox}} + V_{fb} \qquad \text{where} \quad \phi_b = \frac{kT}{q}\ln\left(\frac{N_A}{N_i}\right)$$

Ideal threshold voltage ($2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_b}}{C_{ox}}$); Flat band voltage ($V_{fb}$); Bulk potential ($\phi_b$)

and

N_A: Density of the carriers in the doped semiconductor substrate.

N_i: The carrier concentration of intrinsic (undoped) silicon.

$$N_i = 1.45 \times 10^{10} cm^{-3} \text{ (at 300 degrees K)}$$

k: Boltzman's constant. T: temperature. q: electronic charge.

$$\frac{kT}{q} = 25mV \text{ (at 300 degrees K)}$$

ε_{Si}: permittivity of silicon

$$\varepsilon_{Si} = 1.06 \times 10^{-12} \text{ Farads/cm}$$

C_{ox}: gate-oxide capacitance.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Threshold Voltage

Threshold voltage (cont.):

$$V_t = 2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_b}}{C_{ox}} + V_{fb}$$

Ideal threshold voltage ($2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_A 2\phi_b}}{C_{ox}}$) — Flat band voltage ($V_{fb}$)

and

$$V_{fb} = \phi_{ms} - \frac{Q_{fc}}{C_{ox}}$$

where Q_{fc} represents the fixed charge due to imperfections in silicon-oxide interface and doping.

and ϕ_{ms} is work function difference between gate material and silicon substrate ($\phi_{gate} - \phi_{Si}$).

Typical values of V_{fb} for n/p transistor is **-0.9V** (with $N_A = 10^{16}$ cm^{-3}) and **-0.2V**. (See text for examples).

Typical values of V_t for n and p-channel transistors are +/- 700mV.

Threshold Voltage

From equations, threshold voltage may be varied by changing:

- The doping concentration (N_A).
- The oxide capacitance (C_{ox}).
- Surface state charge (Q_{fc}).

As you can see, it is often necessary to adjust V_t.

Two methods are common:

- Change Q_{fc} by introducing a small doped region at the oxide/substrate interface via ion implantation.

- Change C_{ox} by using a different insulating material for the gate.

  A layer of Si_3N_4 (silicon nitride) with a relative permittivity of 7.5 is combined with a layer of silicon dioxide (relative permittivity of 3.9).

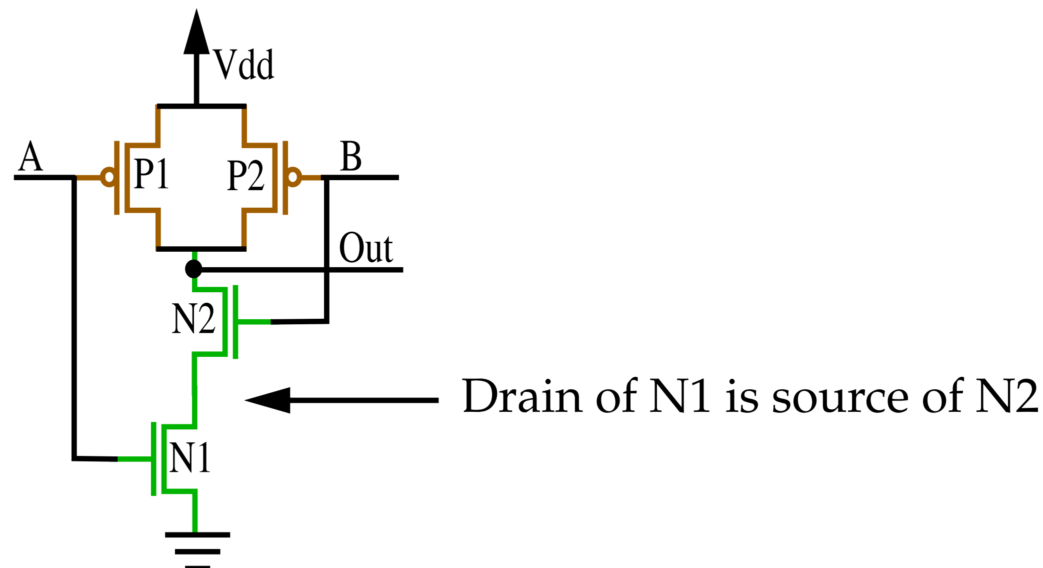
  This results in a relative permittivity of about 6.

  For the same thickness dielectric layer, C_{ox} is larger using the combined material, which lowers V_t.

Body Effect

In digital circuits, the substrate is usually held at zero.

The sources of n-channel devices, for example, are also held at zero, except in cases of series connections, e.g.,



The source-to-substrate (V_{sb}) may increase at this connections, e.g. $V_{sbN1} = 0$ but V_{sbN2} /= 0.

V_{sb} adds to the channel-substrate potential:

$$V_t = 2\phi_b + \frac{\sqrt{2\varepsilon_{Si} q N_A |2\phi_b + V_{sb}|}}{C_{ox}} + V_{fb}$$

Basic DC Equations

Ideal first order equation for *cut-off* region:

$$I_{ds} = 0 \quad \text{when} \quad V_{gs} \le V_t$$

Ideal first order equation for *linear* region:

$$I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \quad \text{when} \quad 0 < V_{ds} < V_{gs} - V_t$$

Ideal first order equation for *saturation* region:

$$I_{ds} = \beta\frac{(V_{gs} - V_t)^2}{2} \quad \text{when} \quad 0 < V_{gs} - V_t \le V_{ds}$$

with the following definitions:

$$\beta = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)$$

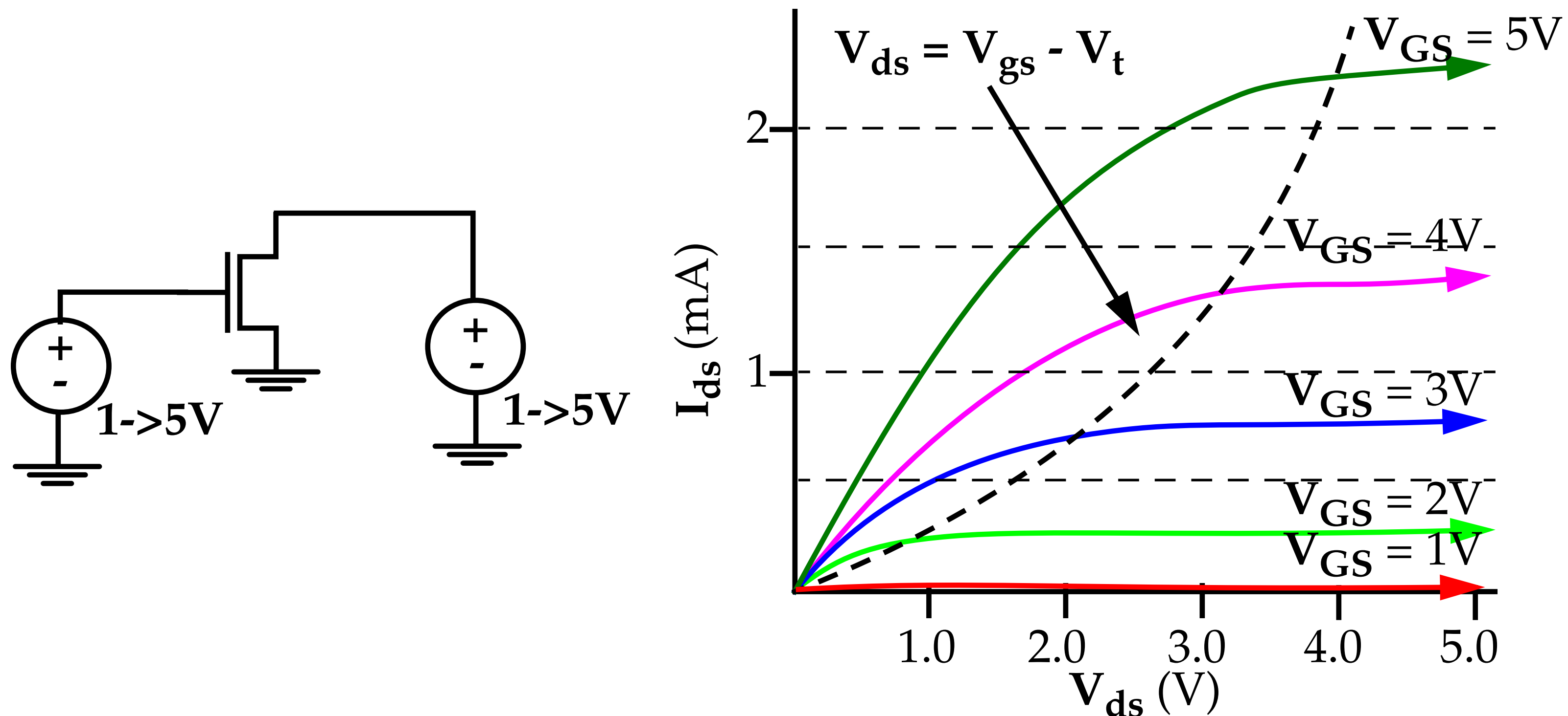
μ = surface mobility of the carriers.
ε = permittivity of the gate insulator.
t_{ox} = thickness of the gate insulator.
W and L are the width and length of channel.

Basic DC Equations

Process dependent factors: $\frac{\mu\varepsilon}{t_{ox}}$ or μC_{ox} where $C_{ox} = \frac{\varepsilon}{t_{ox}}$.

Geometry dependent factors: W and L.

Voltage-current characteristics of the n- and p-transistors.



Beta calculation

Transistor beta calculation example:

Typical values for an n-transistor in 1 micron technology:

$$\mu_n = 500\text{cm}^2/\text{V-sec}$$

$$\varepsilon = 3.9\varepsilon_0 = 3.9 \times 8.85{\times}10^{-14}\text{F/cm}$$ (permittivity of silicon dioxide)

$$t_{ox} = 20\text{nm}$$

Compute beta:

$$\beta_n = \frac{500 \times 3.9 \times 8.85{\times}10^{-14}}{0.2{\times}10^{-5}} \frac{W}{L} = 86.3 \frac{W}{L} \mu A / V^2$$

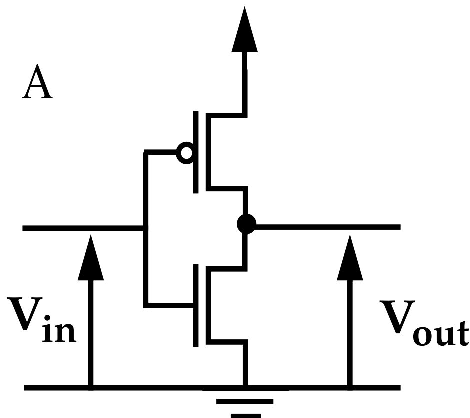
How does this beta compare with p-devices:

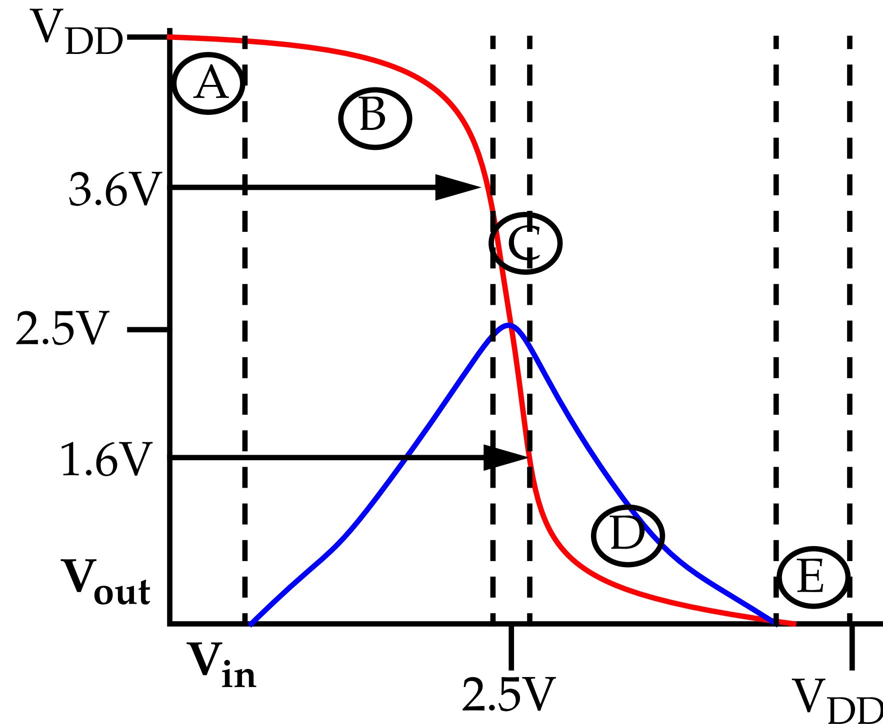
$$\beta_p = \frac{180 \times 3.9 \times 8.85{\times}10^{-14}}{0.2{\times}10^{-5}} \frac{W}{L} = 31.1 \frac{W}{L} \mu A / V^2$$

n-transistor gains are approximately 2.8 times larger than p-transistors.

Inverter voltage transistor characteristics

Inverter DC characteristics





(A) $0 \le V_{in} \le V_{tn}$;n-device is cut off (I_{dsn}=0), p-device in linear.

(B) $V_{tn} < V_{in} < V_{DD}/2 - \Delta$;n-device is in sat., p-device in linear.

(C) $V_{DD}/2 - \Delta \le V_{in} \le V_{DD}/2 + \Delta$;n-device is in sat., p-device in sat.

(D) $V_{DD}/2 + \Delta < V_{in} < V_{DD} + V_{tp}$;n-device is in linear, p-device in sat.

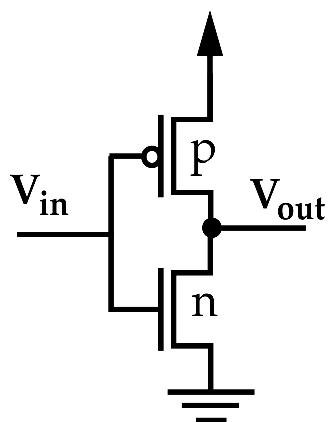
(E) $V_{DD} + V_{tp} \le V_{in} \le V_{DD}$;n-device is in linear, p-device in cut off (I_{dsp}=0).

Beta Ratios

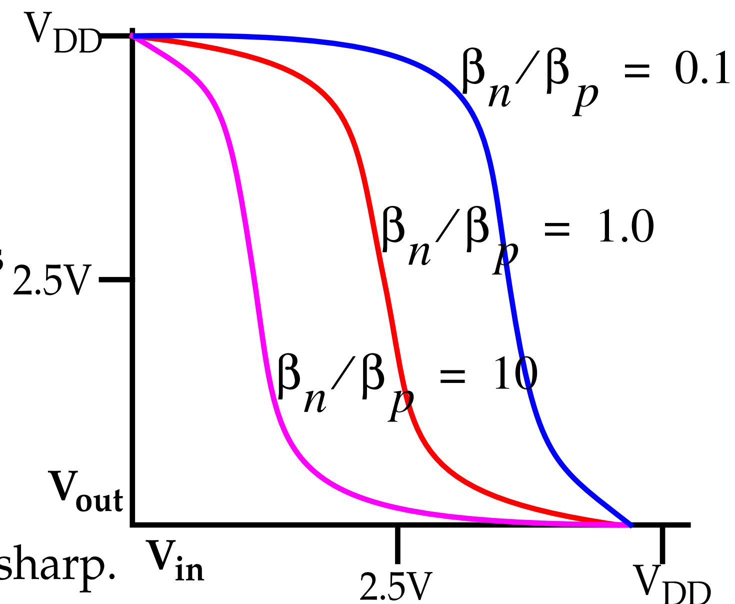
Region C is the most important region. A small change in the input voltage, V_{in}, results in a LARGE change in the output voltage, V_{out}.

This behavior describes an amplifier, the input is amplified at the output. The amplification is termed transistor gain, which is given by beta.

Both the n and p-channel transistors have a beta. Varying their ratio will change the characteristics of the output curve.



Beta ratio of n and p-channel transistors varied over two orders of magnitude.



As ratio is decreased, curve shifts to the right, but the output transition remains sharp.

Beta Ratios

Therefore, the

$$\frac{\beta_n}{\beta_p}$$

does NOT affect switching performance.

What factor would argue for a ratio of 1 for $\frac{\beta_n}{\beta_p}$?

Load capacitance !

The time required to charge or discharge a capacitive load is equal when

$$\frac{\beta_n}{\beta_p} = 1 .$$

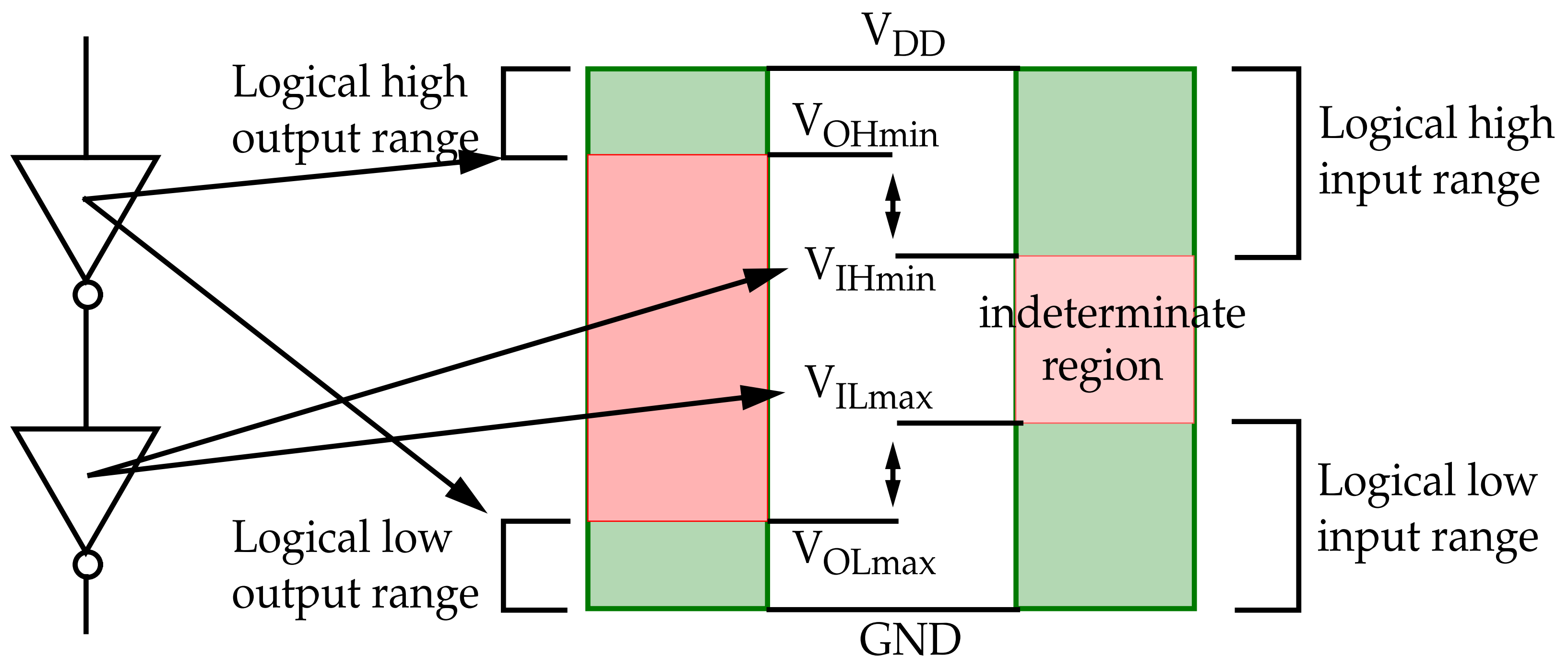
Since beta is dependent W and L, we can adjust the ratio by changing the sizes of the transistor channel widths, by making p-channel transistors **wider** than n-channel transistors.

Noise Margins

A parameter that determines the maximum **noise** voltage on the input of a gate that allows the output to remain stable.

Two parameters, Low noise margin (NM_L) and High noise margin (NM_H).

NM_L = difference in magnitude between the max LOW output voltage of the driving gate and max LOW input voltage recognized by the driven gate.

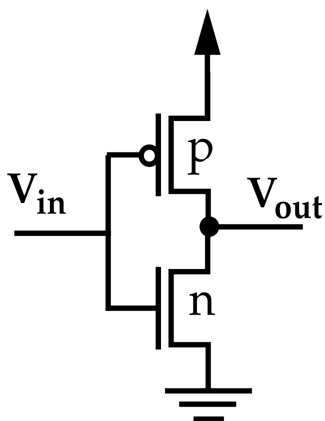


Noise Margins

Ideal characteristic: $V_{IH} = V_{IL} = (V_{OH}+V_{OL})/2$.

This implies that the transfer characteristic should switch abruptly (high gain in the transition region).

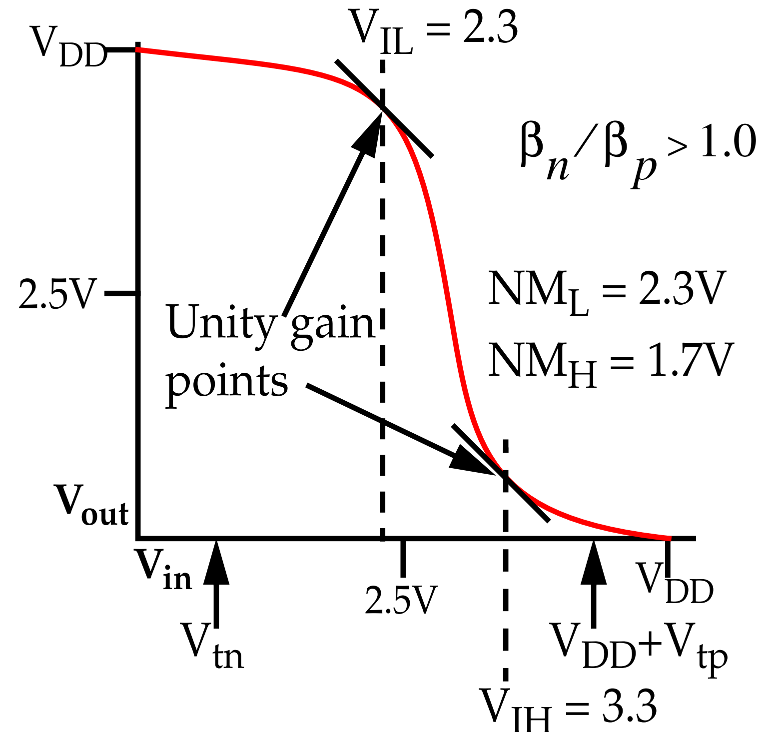
V_{IL} found by determining unity gain point from V_{OH}.



Assume output of driving gate is stable at supply voltage, e.g.,

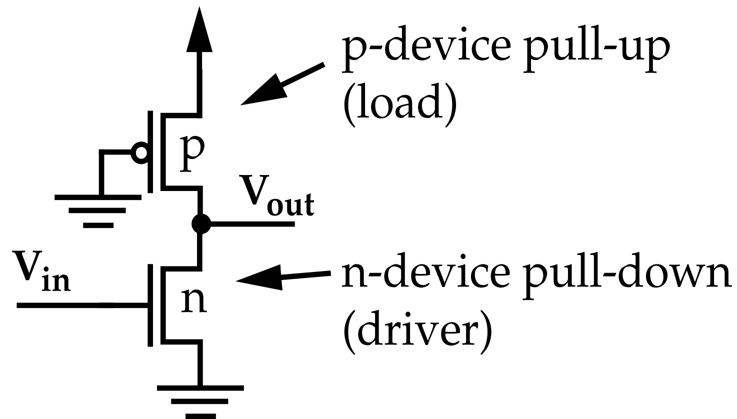
$V_{OH} = 5V$

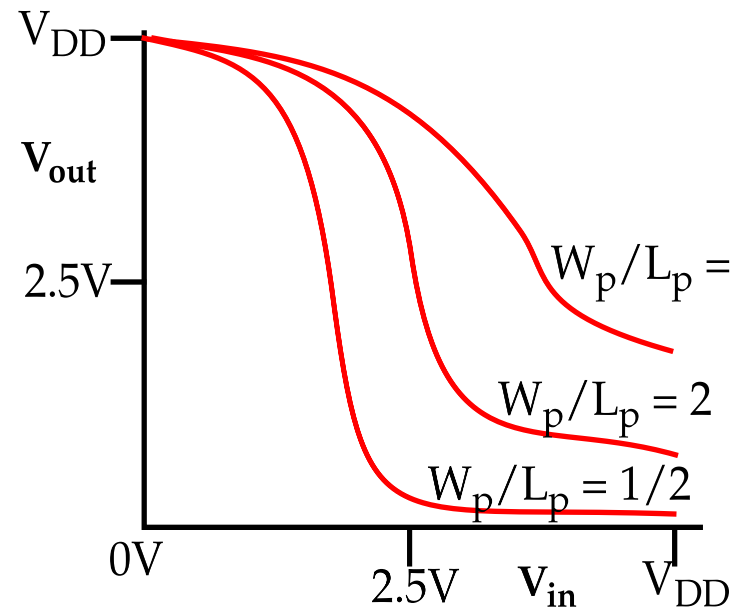
$V_{OL} = 0V$



Noise margins are often compromised to improve speed.

Pseudo-nMOS Inverter





When driver is on, steady-state current flows - not a good choice for low-power circuits.

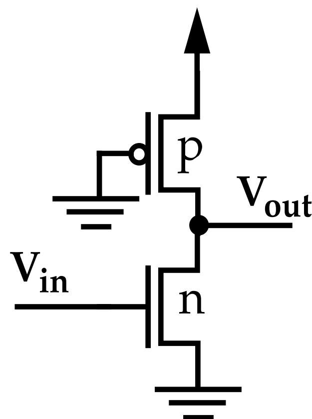
Therefore, the shape of the transfer characteristic and the V_{OL} of the inverter is affected by the ratio $\frac{\beta_n}{\beta_p}$.

In general, the low noise margin is considerably worse than the high noise margin for Pseudo-nMOS.

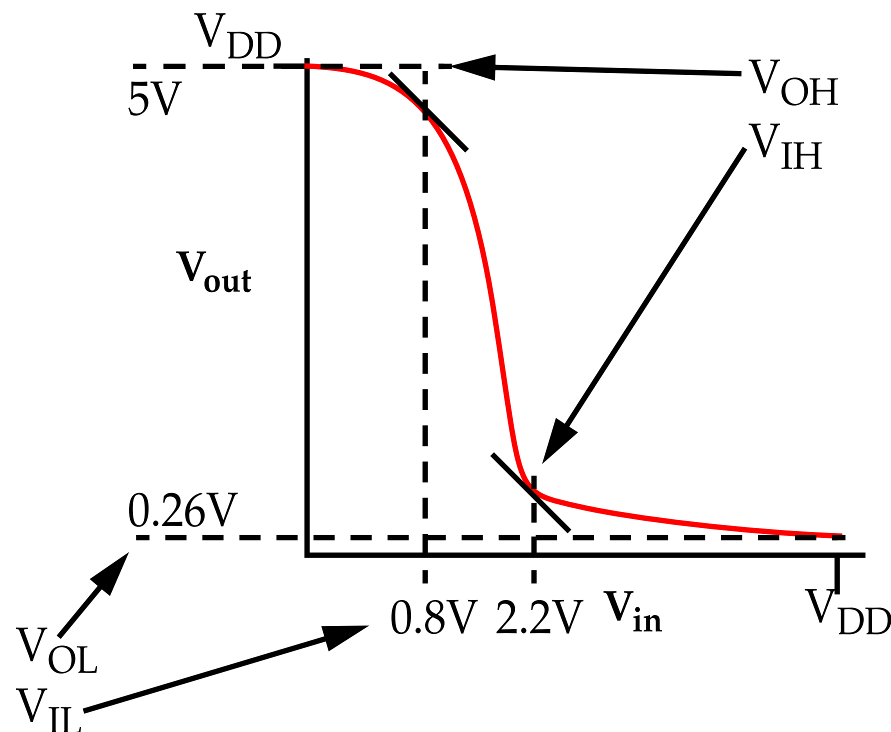
Pseudo-nMOS was popular for high-speed circuits, static ROMs and PLAs.

Pseudo-nMOS

Example: Calculation of noise margins:



Pseudo-nMOS inverter



$NM_H = V_{OH} - V_{IH} = 5V - 2.2V = 2.8V$

$NM_L = V_{IL} - V_{OL} = 0.8V - 0.26V = 0.54V$ (This is quite a bit worse than NM_H)

The transfer curve for the pseudo-nMOS inverter can be used to calculate the noise margins of identical pseudo-nMOS inverters.