CMOS Processing Technology

Silicon: a semiconductor with resistance between that of conductor and an insulator.

Conductivity of silicon can be changed several orders of magnitude by introducing **impurity atoms** in silicon crystal lattice.

- Impurities that *use* electrons: acceptors (p-type), e.g., Boron.
- Impurities that *provide* electrons: donors (n-type), e.g., Phosphorous.

Wafer: 75mm to 230mm (~3″ to ~9″) and 0.25mm to 1mm thick.

Oxidation: Formation of glass or SiO_2.

Wet Oxidation uses water vapor and **Dry Oxidation** uses pure oxygen.

SiO_2 growth consumes silicon, grows into the substrate.

SiO_2 is twice the volume of Si, projects above the substrate as well.

CMOS Processing Technology

Epitaxy, Ion-Implantation and Deposition/Diffusion: Ways of introducing impurities into pure silicon.

- **Epitaxy**: Single-crystal film grown on silicon surface.
- **Deposition**: Evaporate dopant material onto surface, high temps drive impurities into silicon bulk (diffusion).
- **Ion implantation**: Highly energized donor and acceptor atom driven into the silicon.

How much dopant that is introduced is controlled by energy and amount of time.

Where it is introduced is controlled by masks (thin films of special material).
Mask materials include:

photoresist
polysilicon
silicon dioxide (SiO_2)
silicon nitride (SiN)

CMOS Processing Technology

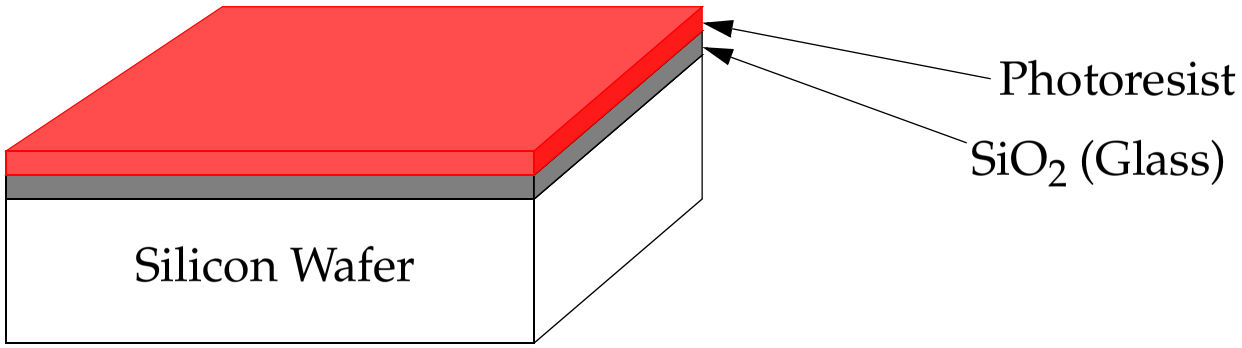
Selective diffusion: Masks act as a barrier to prevent impurities from diffusing.

Process involves:

- Patterning windows in the mask on the die surface.
- Introducing impurities in exposed regions.
- Removing the mask.

For example, to cut windows into the glass after oxidation step:

Acid resistant coating (photoresist) spread evenly on surface.



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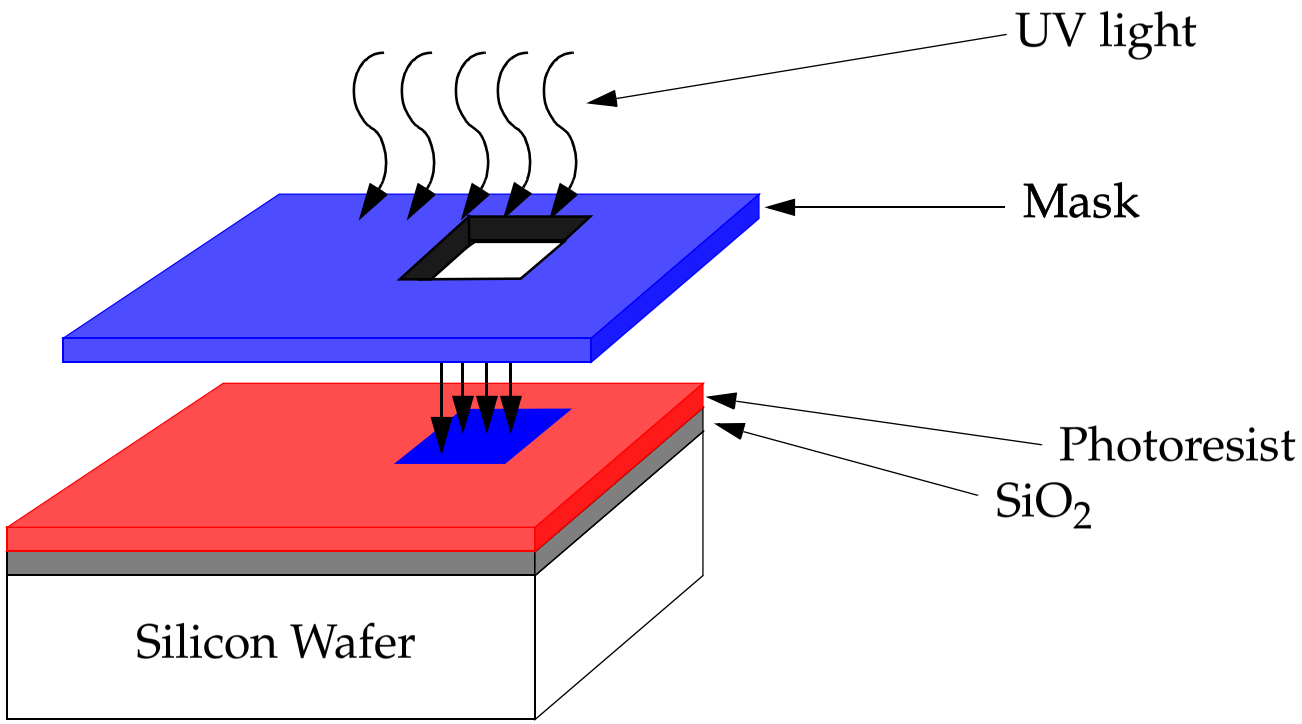
Polymerized in areas exposed by UV light.



Mask controls region exposed.

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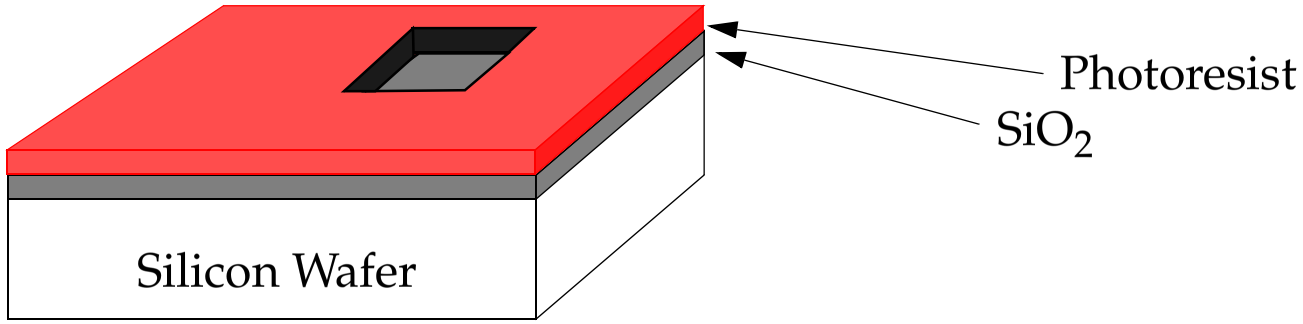
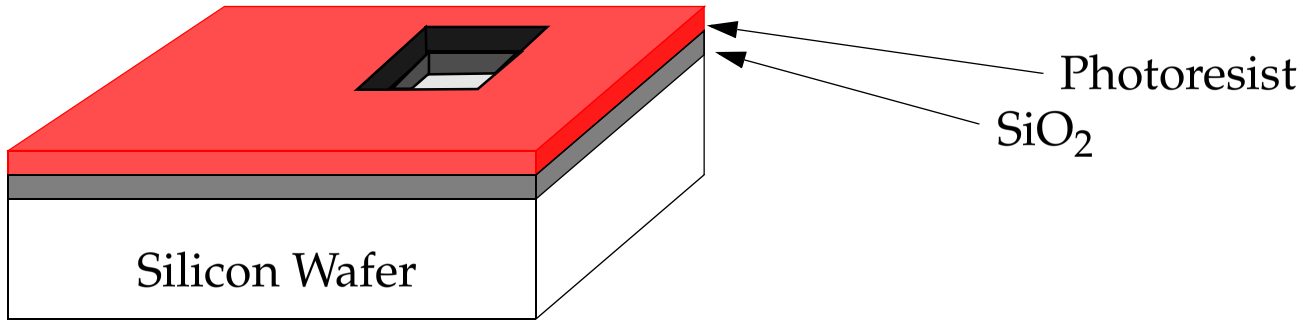
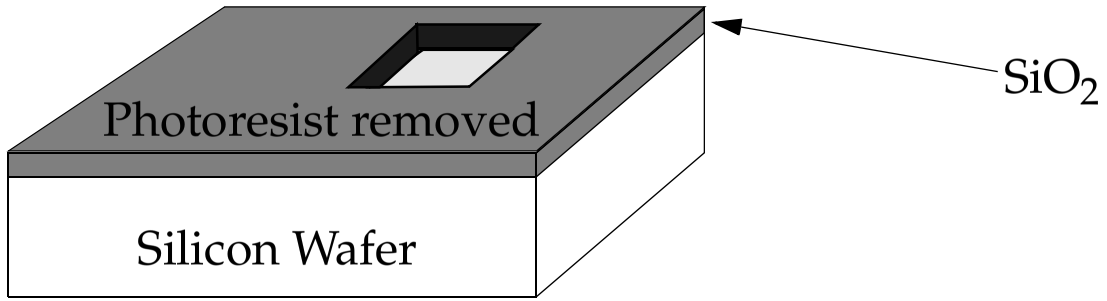
Organic solvent removes polymerized areas.



Windows are etched using an acid and the photoresist is removed.





CMOS Processing Technology

Positive resist: Exposed photoresist removed.

Negative resist: Unexposed photoresist removed.

UV light defraction and alignment tolerances limit line widths to ~0.8microns.

Electron beam lithography: Reduces line width limits to 0.5microns.

Adv:

- No intermediate hardware images such as masks.
- Changes to patterns can be implemented immediately.

Disadv:

- Cost of equipment is high.
- Requires large amount of time to process each wafer.

CMOS Processing Technology

Polysilicon: A polycrystalline (not a single crystal) form of silicon.

Used as:

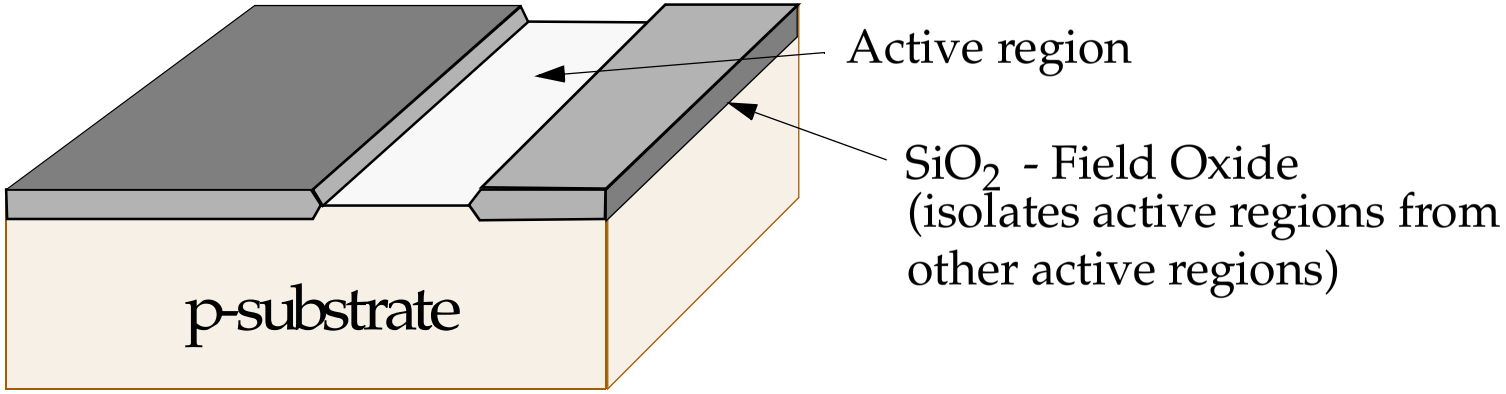
- Interconnection material.
- Gate electrodes.
- *** A mask to allow precise definition of source and drain ***.

Undoped poly has a very high resistance.

Poly and the source/drain regions are usually doped at the same time.

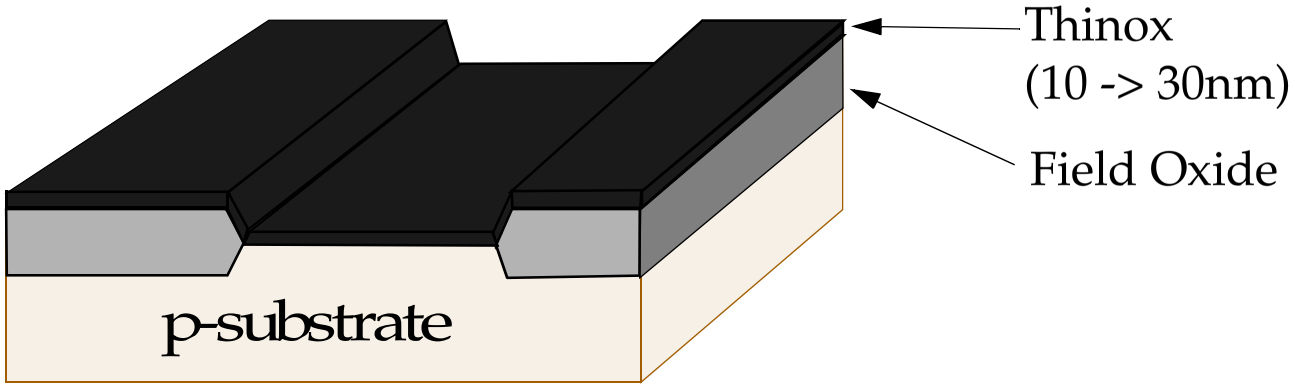
Silicon Gate Process:

Oxidation and etching of the active region:

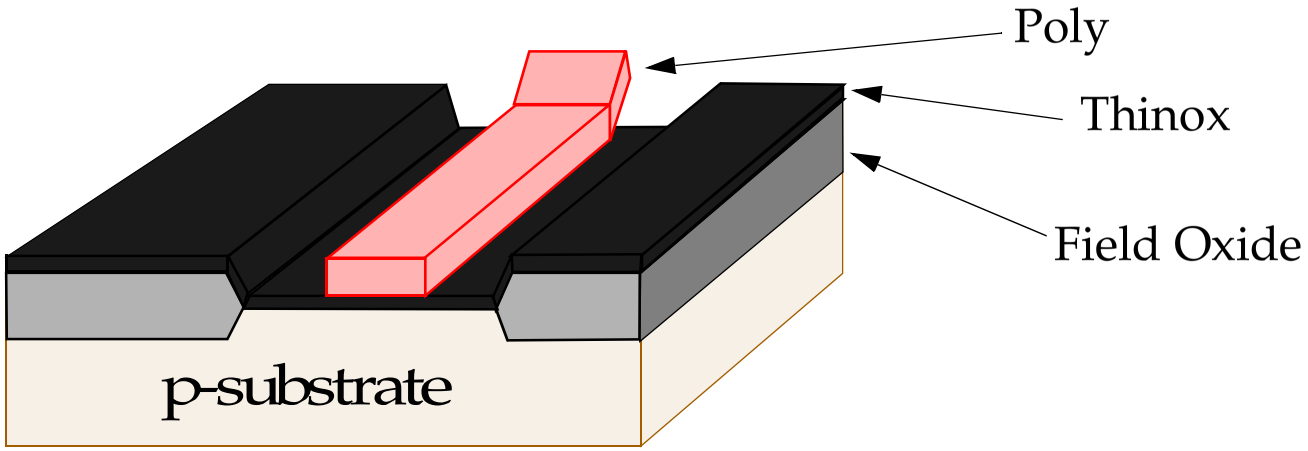


CMOS Processing Technology

Thin Oxide grown:



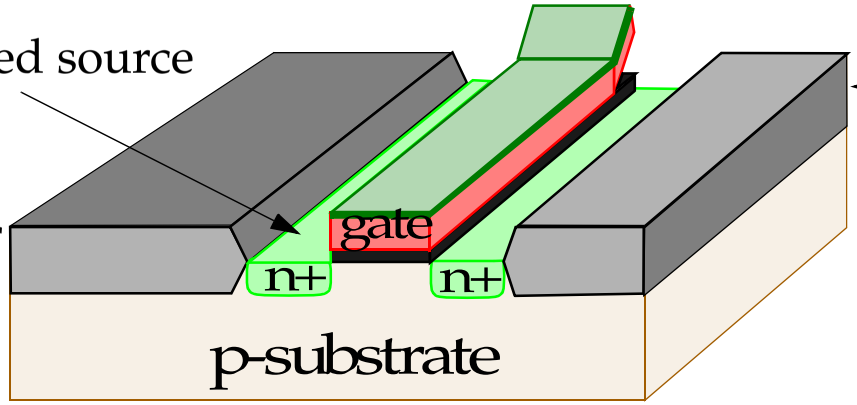
Polysilicon deposited and etched:



CMOS Processing Technology

Etching of thinox and dopant Ion-Implantation or Deposition/Diffusion:

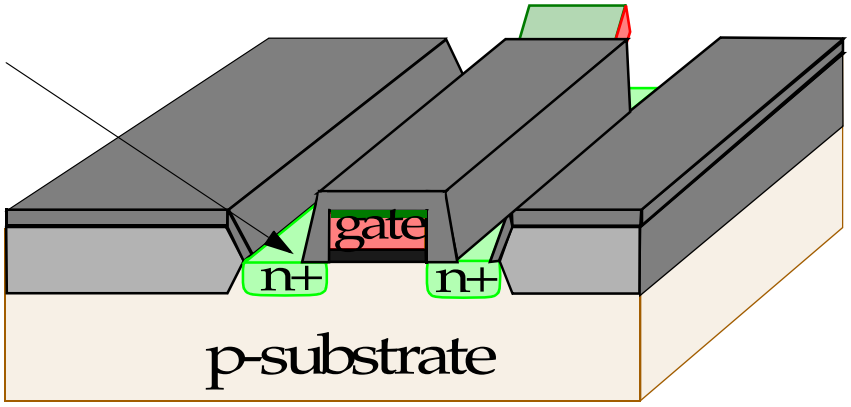
*** Self-aligned source and drain *** do NOT extend under the gate.



Field Oxide

SiO_2 and contact cuts.

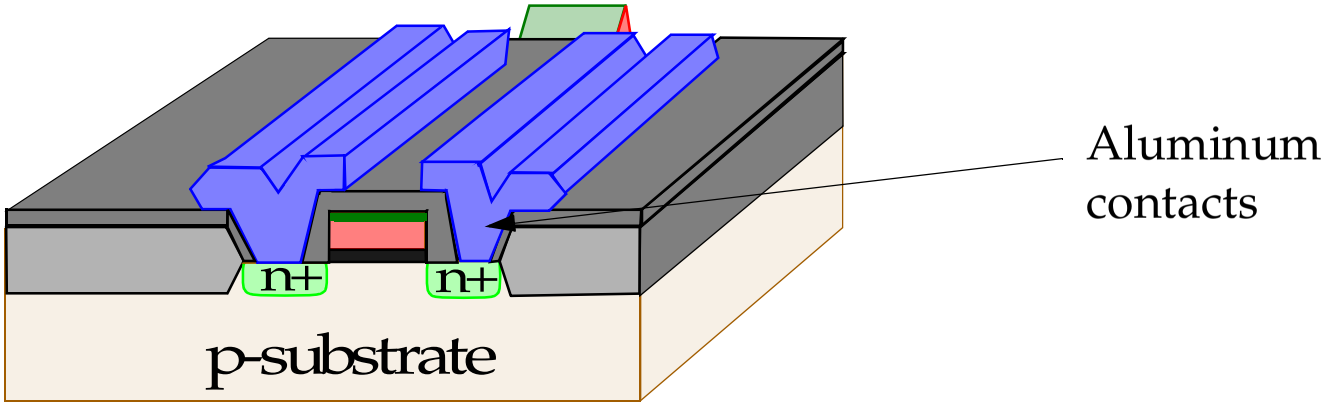
Contact cuts



SiO_2

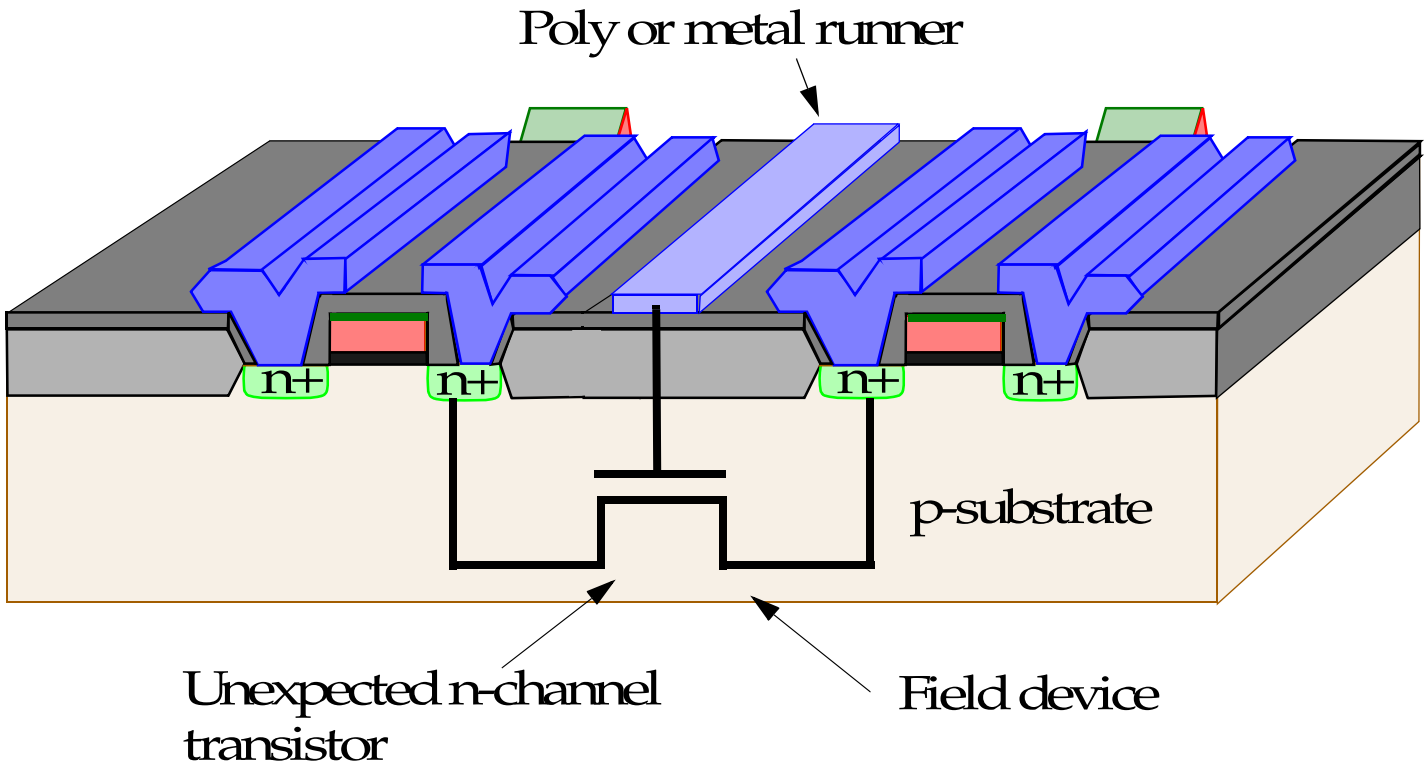
CMOS Processing Technology

Aluminum evaporated and etched:



CMOS Processing Technology

Parasitic MOS transistor:



Field device Countermeasures:

Make the **threshold voltage** of field device high by:

- Making the field oxide thick.
- Introducing a "channel-stop" diffusion (higher impurity concentration).

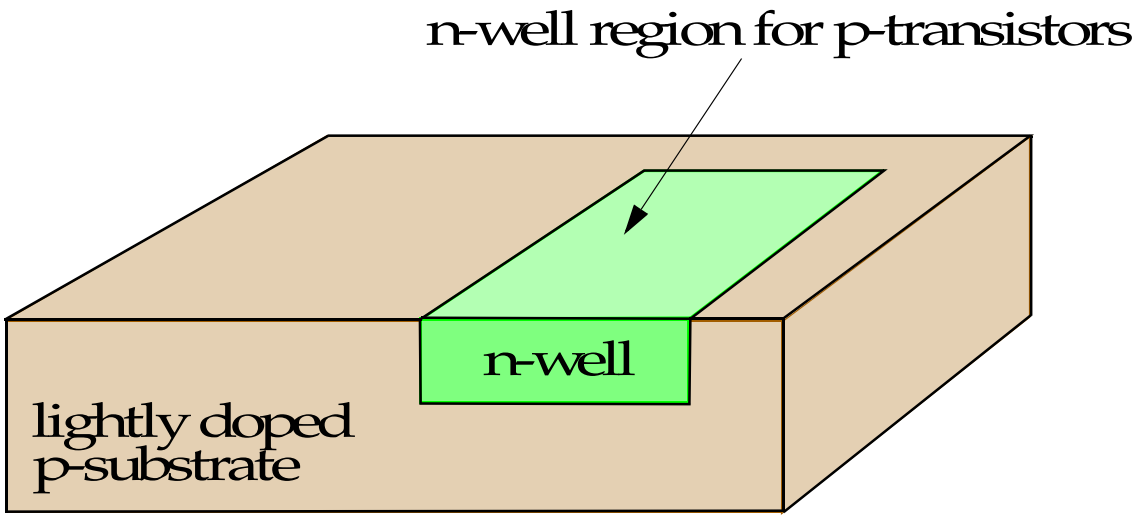
CMOS Processing Technology

Four main CMOS technologies:

- n-well process
- p-well process
- twin-tub process
- silicon on insulator

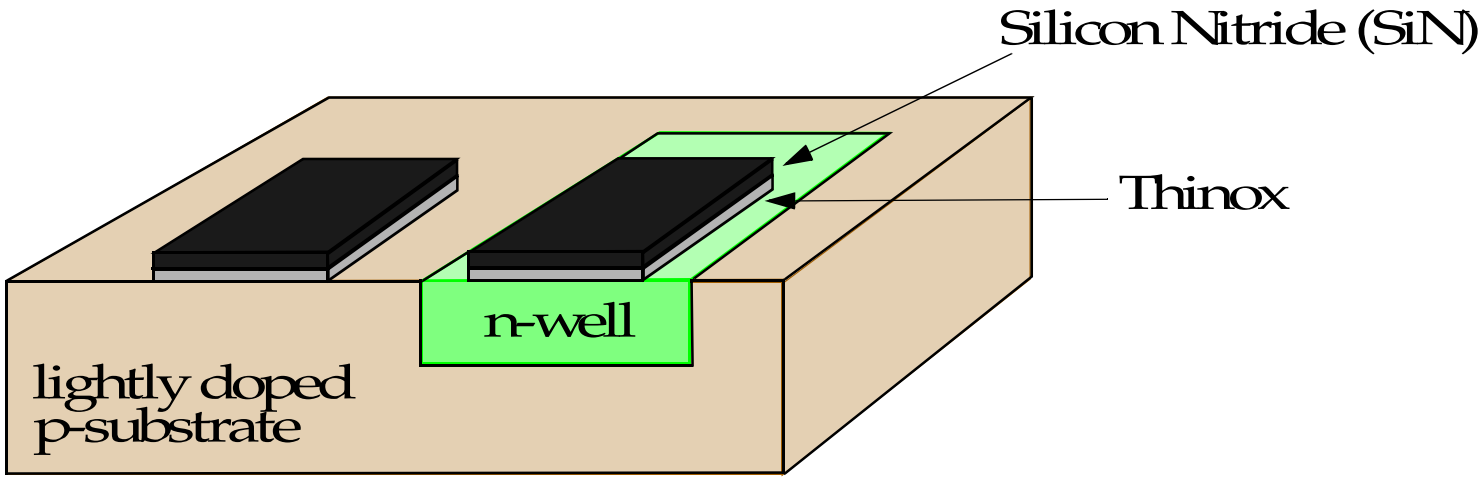
Major process steps of n-well process:

- *n-well mask* used to create n-well or n-tub via ion-implantation or deposition/diffusion.

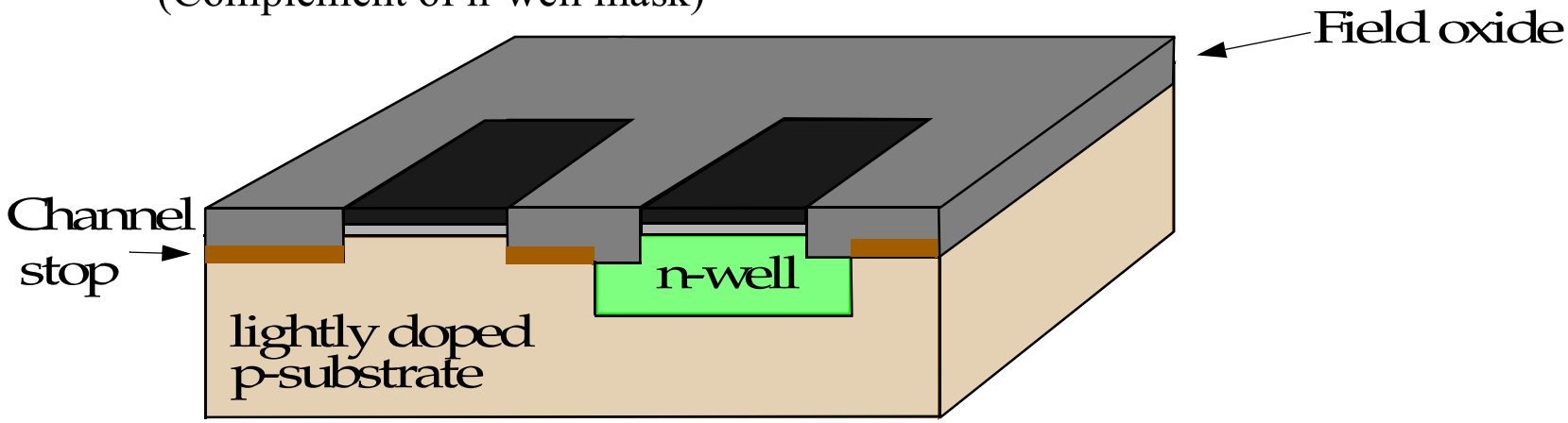


CMOS Processing Technology

- *active mask* defines areas where transistors are fabricated.

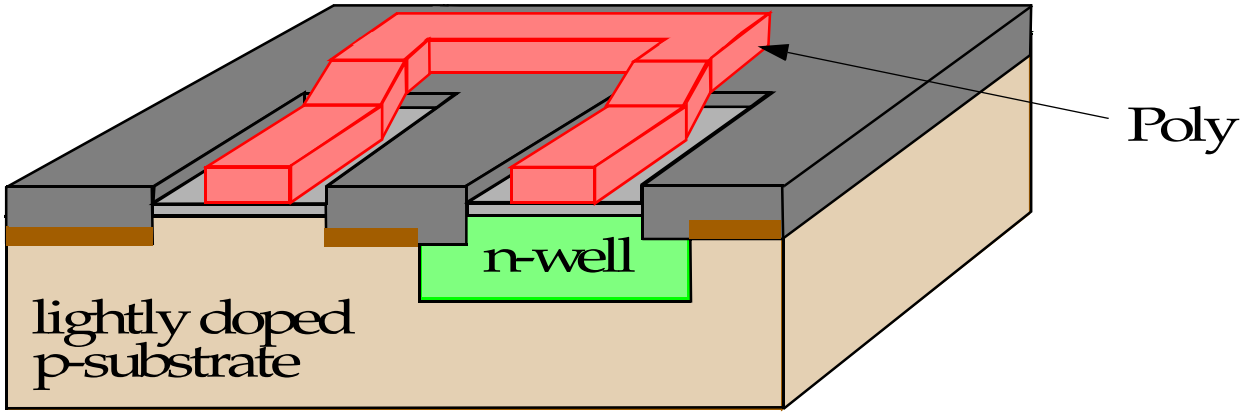


- *p-well mask* used to produce channel-stop (p^+ diffusion), field oxide grown.
  (Complement of n-well mask)

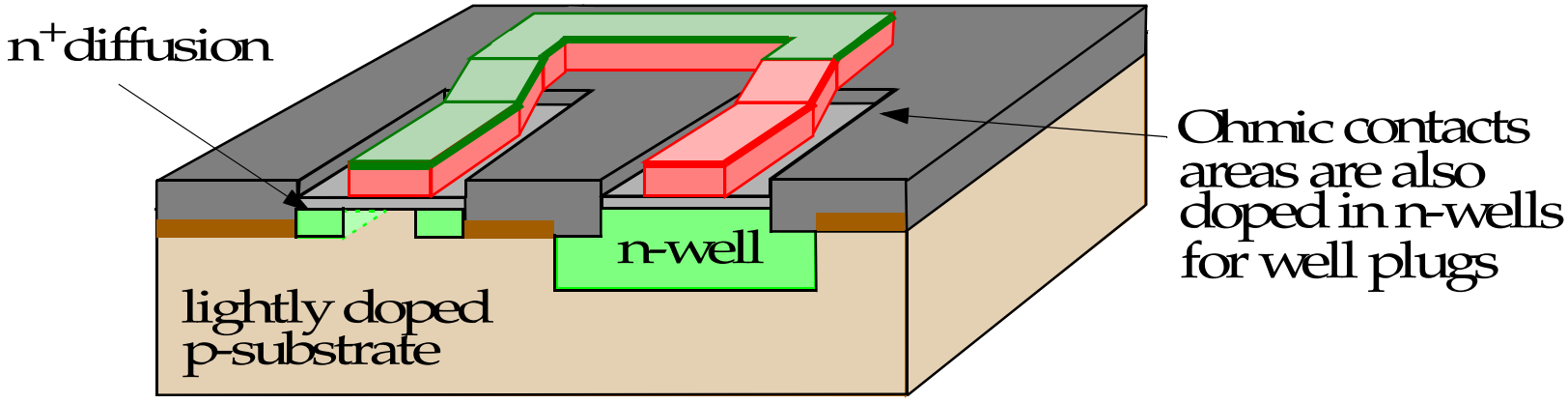


CMOS Processing Technology

- *poly mask* used to etch poly patterns.

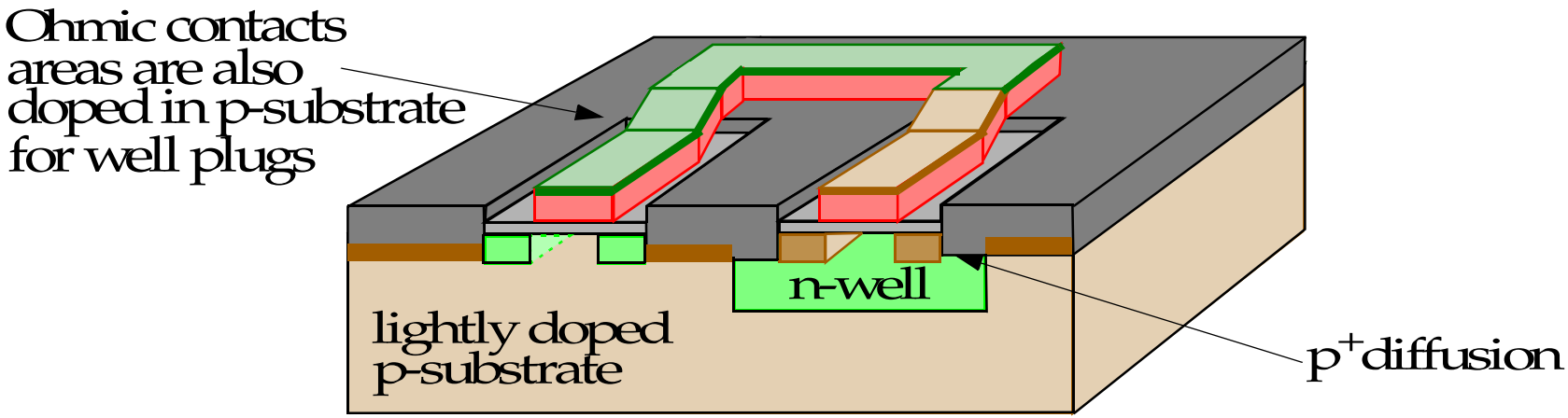


- *n-plus mask* (*select mask*) used to indicate those thin-oxide areas and poly that are to implanted n^+.

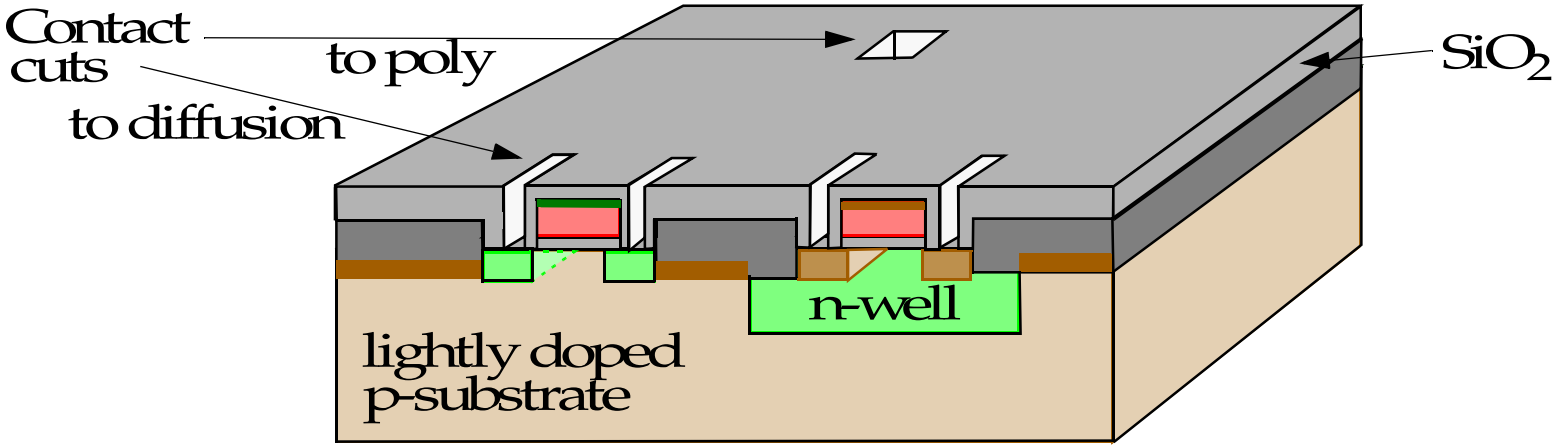


CMOS Processing Technology

- *p-plus mask* used to indicate those thin-oxide areas and poly that are to implanted p^+.

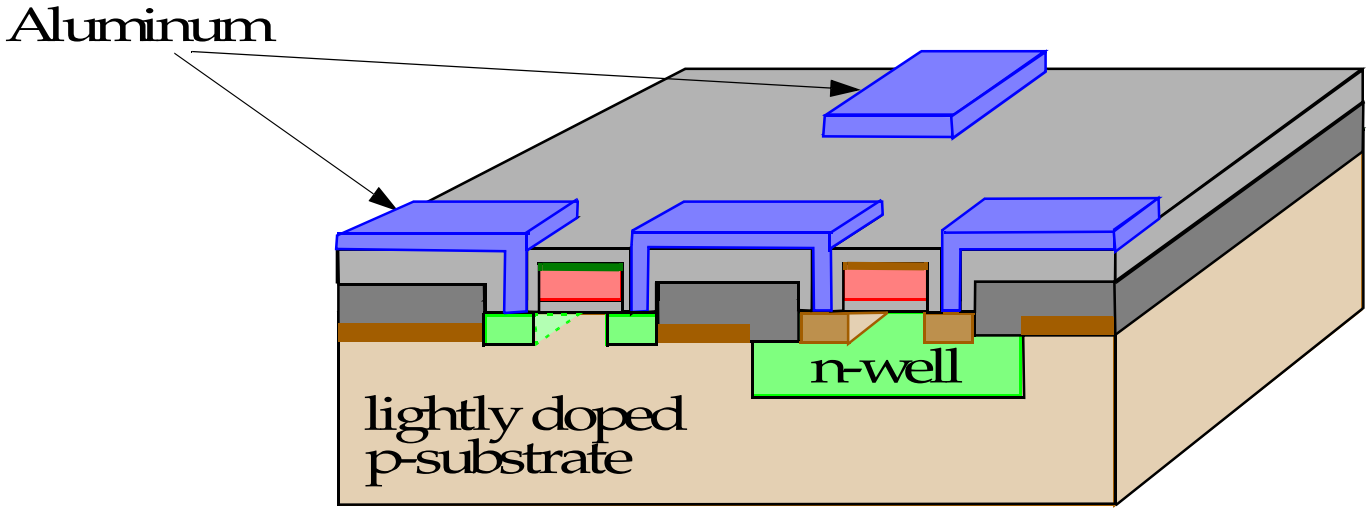


- Surface is covered with SiO_2 and contact cuts made.



CMOS Processing Technology

- Metallization applied and etched using *metal mask*.



- The wafer is then passivated and opening to bond pads are etched.