# CMPE 413/CMSC 613: Principles of VLSI Design

#### **Course:**

CMPE 413/CMSC 613: Principles of VLSI Design, Fall 2000. 4 credits.

### **Course Instructor:**

Dr. Jim Plusquellic, Professor of Computer Science & Electrical Engineering Office: ECS 212, Telephone: 410-455-1349 Email: plusquel@umbc.edu, Home Page: http://www.cs.umbc.edu/~plusquel/ Office Hours: T-Th 5:15-6:30pm or by appointment Teaching Assistant: Chintan Patel, cpatel2@cs.umbc.edu

#### Text:

Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design: A Systems Perspective," Second Edition, Addison Wesley (1993).

# Supplementary text:

Ken Martin, "Digital Integrated Circuit Design", Oxford University Press (2000). Jan M. Rabaey, "Digital Integrated Circuits, A Design Perspective", Prentice Hall (1996).

## Grading:

The distribution of weights for the exams, homeworks and projects is as follows:

Exam 1	15%
Exam 2	15%
Final	20%
Labs/Homework	15%
Project	30%
Class Participation	5%

No incompletes will be given, except as required by university policy for truly exceptional circumstances.

The final exam is cumulative. However, material covered after the second exam will be emphasized.

Students are encouraged to participate in class.

NOTE: Cheating at any time in this course will cause you to fail the course.

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# **Tentative Course Outline:**

Date	Торіс
Sept 6	Introduction and Motivation (Lab: Linux/CADENCE setup/tutorial)
Sept 11	CMOS Technology Characteristics
Sept 13	Modeling Abstractions (Lab: CADENCE Layout)
Sept 18	Details of the MOS Transistor
Sept 20	Details of the MOS Transistor (Lab: CADENCE Spice lab)
Sept 25	Details of the MOS transistor
Sept 27	CMOS Processing Technology (Lab: CADENCE Schematic lab)
Oct 2	Silicon Run I (movie)
Oct 4	Out-of-town (No Lab)
Oct 9	CMOS Processing Technology
Oct 11	Performance Estimation (Lab: CADENCE VHDL)
Oct 16	Performance Estimation
Oct 18	Performance Estimation (Lab: CADENCE Simulation)
Oct 23	Exam I
Oct 25	CMOS Circuit and Logic Design (Lab: Project discussion)
Oct 30	CMOS Circuit and Logic Design
Nov 1	CMOS Circuit and Logic Design (Lab: Project)
Nov 6	Subsystem Design
Nov 8	Subsystem Design (Lab: Project)
Nov 13	Subsystem Design
Nov 15	Modeling and Simulation (Lab: Project)
Nov 20	Modeling and Simulation
Nov 22	Exam II (Lab: Project)
Nov 27	Verification and Testing
Nov 29	Verification and Testing (Lab: Project)
Dec 4	Advanced Topics (time permitting)
Dec 6	Advanced Topics (Lab: Project)
Dec 11	Advanced Topics (Silicon Run II)
Dec 13	Advanced Topics (Lab: Final Project demos and reports due)
Dec 16-22	Final exam

(Note: Changes/Additions to this schedule will be posted on my website http://www.cs.umbc.edu/~plusquel/)