Development of CMOS Standard Cell Library

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Why Create Cell Library?

- Complexity of design continue to increase
- Full-custom design is no longer feasible
- Use of synthesis and Placement-and-Route (PNR) tools has become mandatory
- PNR tools need layout library
- Synthesis tools need logic models of the cells in the layout library, which include timing and power dissipation models

Basic Steps in Standard Cell Based Design

- A description of the system in high-level description language (e.g. VHDL) is created
- The description is synthesized, using synthesis tools, into logical netlist
  - the synthesis tools need logic description of the cells
- The logical netlist is synthesized into physical layout using place-and-route (PNR) tools
  - The PNR tools need layout library and probably also simplified representation of layout

Steps in Library Development

- Creation of layout library
- Circuit level characterization of cell timing and power dissipation parameters
  - timing and power model may be tool-dependent
- Porting the results to the format appropriate for use with the high-level synthesis tool

Layout Library

- PNR tools generate hierarchical layouts
- Layouts in the library comprise the leaf cells
- Shapes must be regularized to facilitate PNR tools in placing cells and routing wires among them
- Has to satisfy requirements imposed by the tools used – again, tool dependent
  - could be more of a handicraft than a science

Requirements Imposed by Tools

- "Functional" completeness: usually must include Flip-flop and Latch (both with Async Set/Reset), tristate buffer, inverter, either (AND and OR) or (NAND and NOR)
- Model library characterized for delay, power dissipation, input capacitance, and for tristate elements also output capacitance
- VHDL/Verilog models and list of pins showing pin directions (input, output, inout)

Wish List for Low-Power Libraries

- Should include cells with varying drive strength (“maximum fanout”)
- Should include double-edge triggered flip-flops, even if they are (as usually?) not supported by the synthesis tool used (after Laurent and Briet ’99)

CMOS Circuit Style Consideration (I)

- Static complementary CMOS is slow and power-hungry at high voltages, but performs well at low V_{DD}, and robust toward noise and incorrect transistor scaling
- Dynamic logic styles are probably the fastest style, small, and may consume less power at higher V_{DD}, but does not respond as well toward V_{DD} reduction and may preclude clock gating
- Pass-transistor and transmission-gate based circuits are often said to be fast and power-saving, but do not function well at low supply voltages

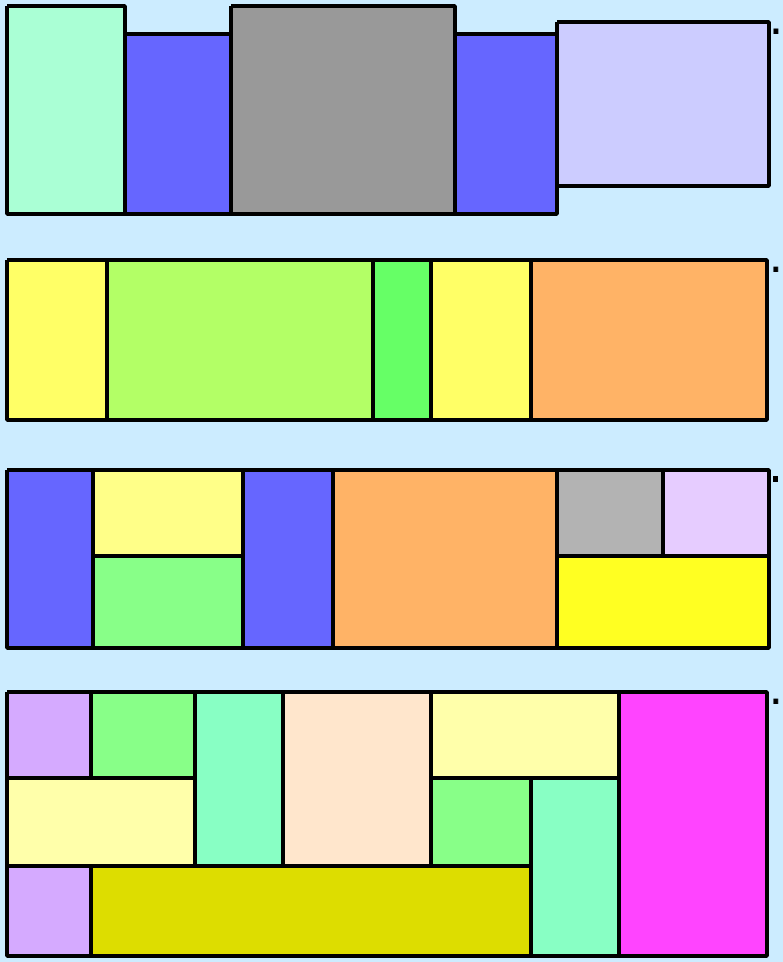
CMOS Circuit Style Consideration (II)

- Except perhaps for XOR-type structures, pass- / transmission-gate structures tend to need too many transistors and buffering – possibly excessive switching power
- If clock gating is practical or or V_{DD} reduction is possible, static complementary CMOS is the hands-down winner for low-power systems
- However, lower supply voltages may not be possible for performance or interoperability reasons

CMOS Circuit Style Consideration (III)

- Various synthesis tools have difficulties with some certain styles, such as pipelined domino logic or styles which requires the presence of complementary inputs
- The presence of static combinational cell in a library is a must for some synthesis tools, even if the sequential cells are dynamic
- In short, various tools need combinational cells which are self contained (i.e. pass-transistor structures which still needs additional buffering may cause trouble)

Layout Style Alternatives – and What They Lead Into



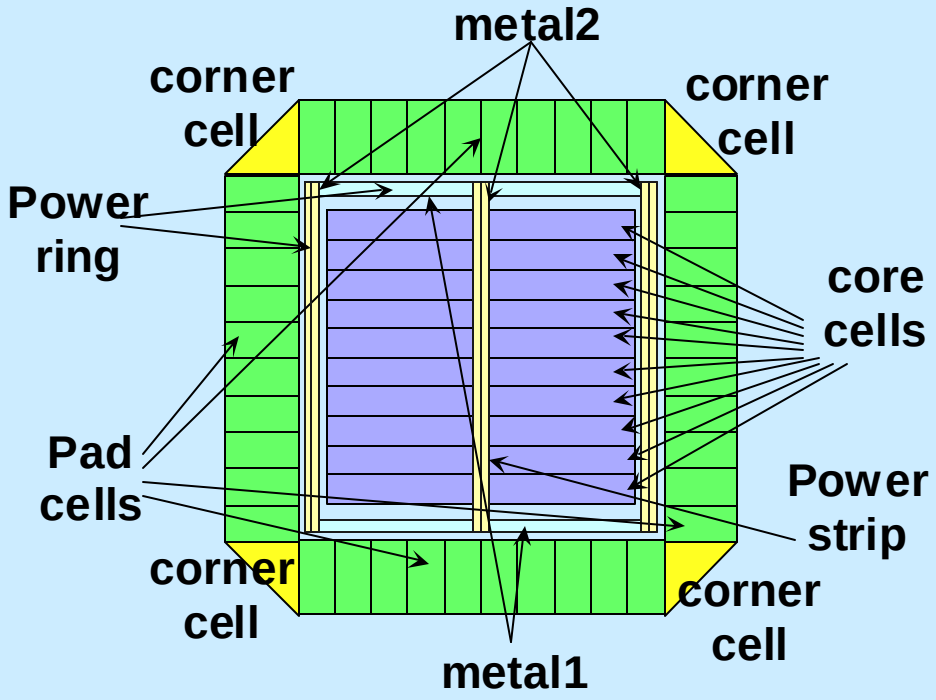
- Different-height cell in one row
  - If only one or two metals are available
  - Otherwise, avoid it!
- Single-height cells in single Row
  - Perhaps the most common
  - The one used here so far
- Single- and double- or multiple-height cells
  - Most efficient, but most complicated

Design Considerations

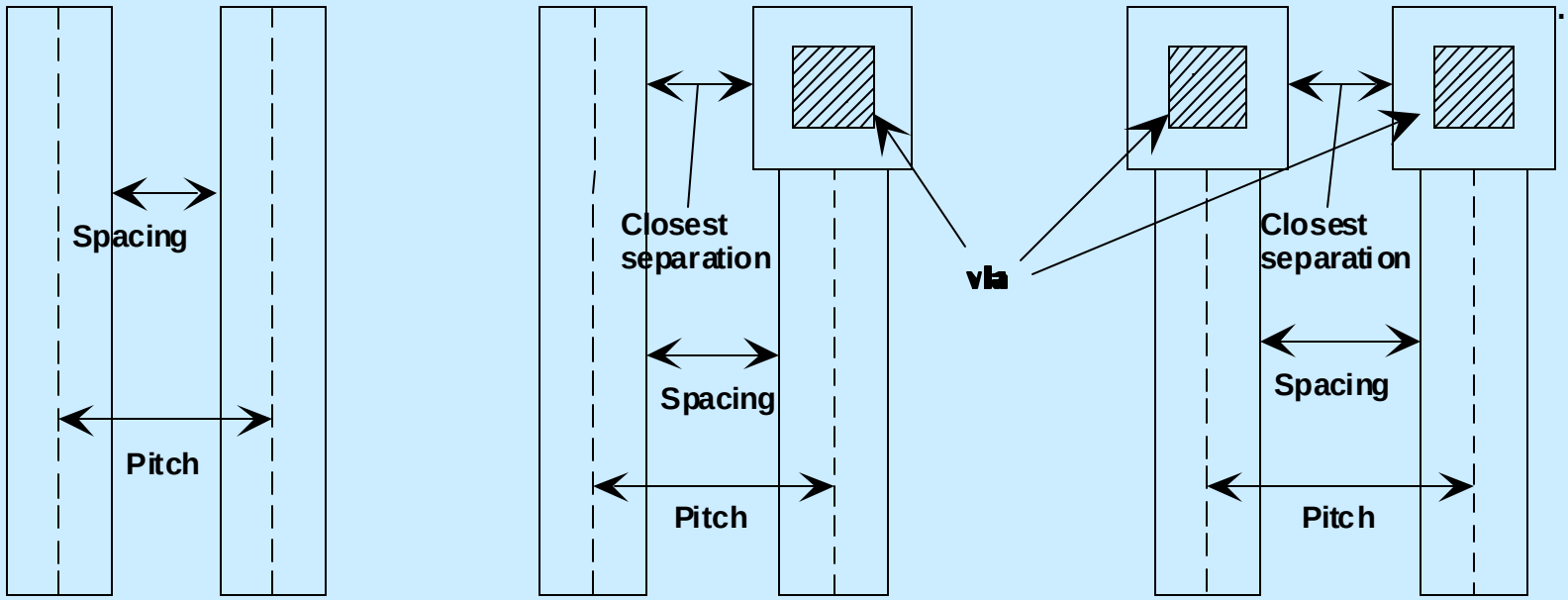
- Design style also depends on tools used
  - Although many PNR tools could use cells of varying heights, not all tools could give accurate estimates of area utilizations for double- or multiple-height cells
  - VTVT group uses single-height cells so far
- Use metal pitch which enables unlimited stacking of via
  - Matters only if stacked via is supported

Typical Silicon Ensemble-Routed Chip

- Cell arranged in abutted rows
- I/O pads placed along the chip perimeter
- Cells in a row may be abutted to each other
- A ring of power and ground connector is placed between pads and core cells



Definition – Pitch: Center-to-Center



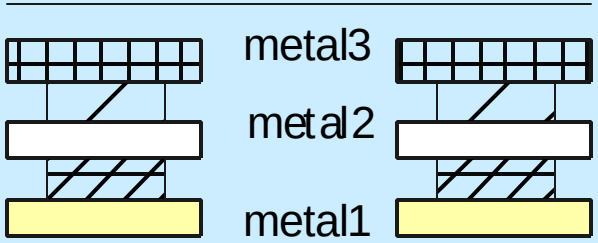
(a). line-to-line pitch

(b). line-to-via pitch

(c). via-to-via pitch

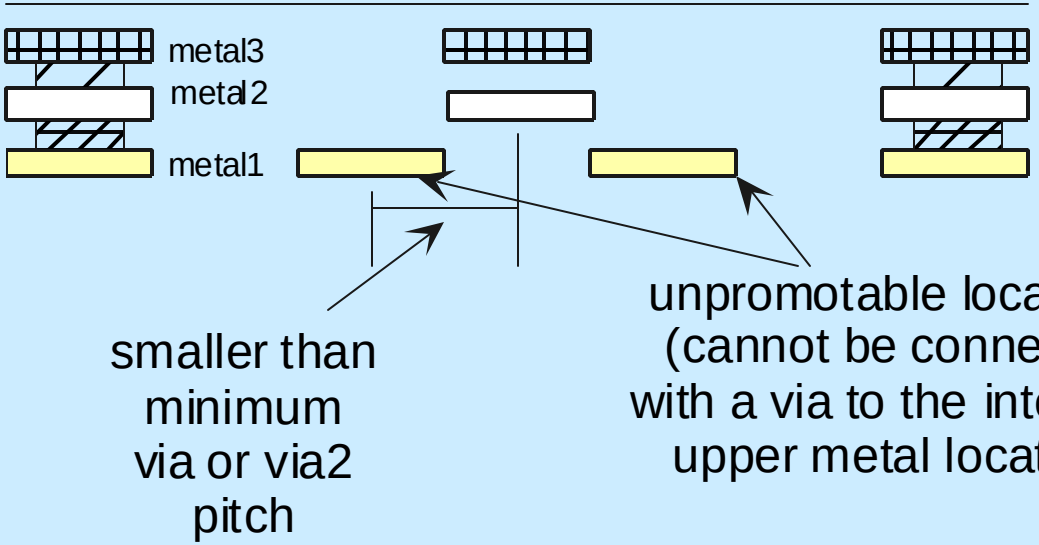
Simple pitch ratios are preferable

1:1 pitch ratio

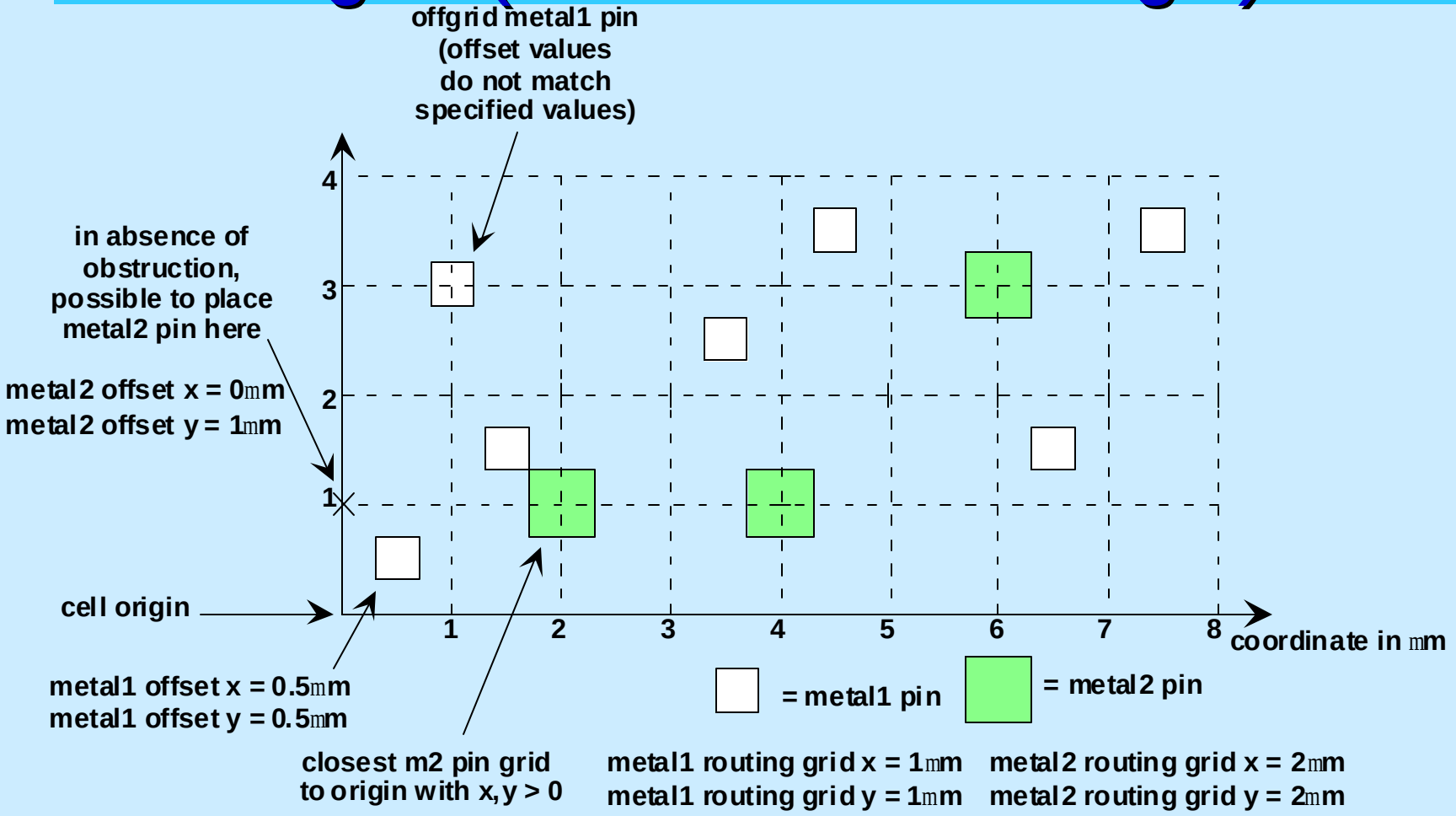


- **Simple pitch ratios facilitate unlimited via stacking**
- **1:1 is ideal; should not be worse than 4:3**

3:2 pitch ratio

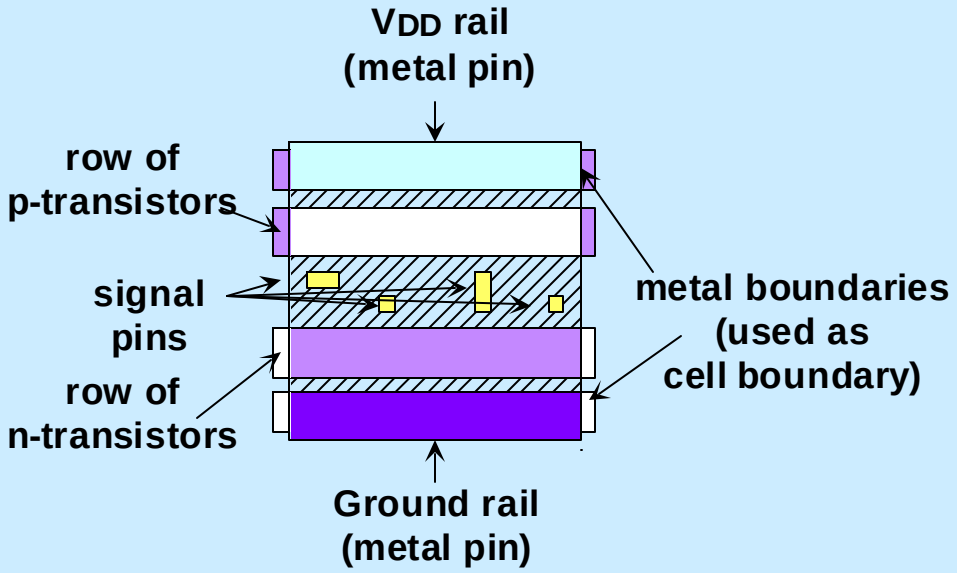


Definition – Offset from Cell Origin (Lower Left Edge)



Basic Cell Shape

- Use single-height style
- All sizes and shapes have to be regularized
- All metal signal tracks in a given layer have to be the same width
- Power and ground tracks must be the same width

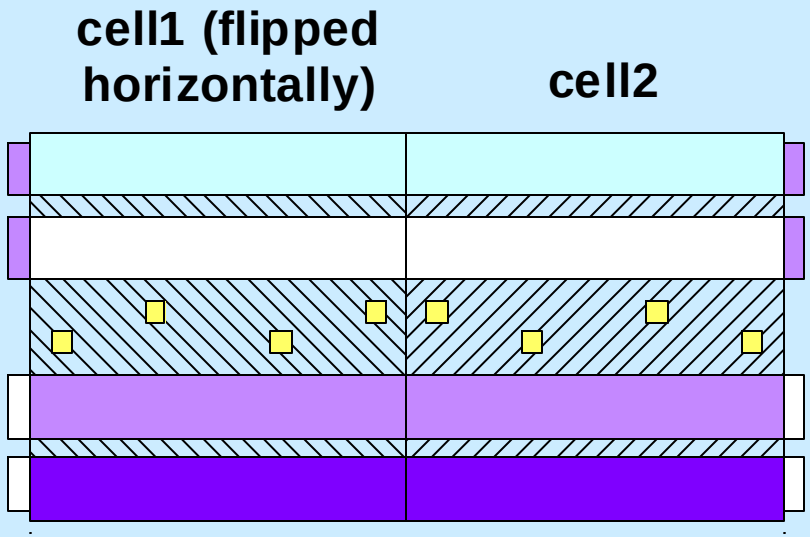


Other Requirements on Cell Shapes

- Use metal1 and metal2 only – leaving upper metals for intercell routing
- Cell width and height must be integer multiple of pitch
- V_{DD}/ground rail width must be the same for all cells
- The V_{DD} and ground rails must have the same horizontal width
- The vertical width of the rails must be the same on both sides (ends) of the cell

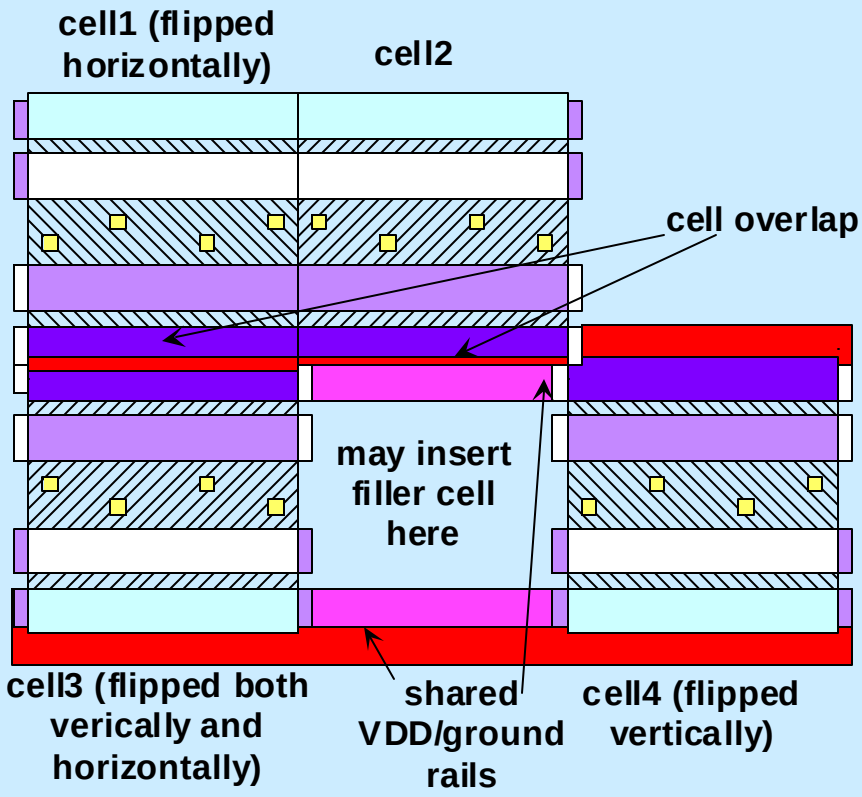
Cell Placement In A Row

- Cells may be flipped horizontally
- VDD of a cell must connect to the VDD of the adjacent cell
  - Same requirement for Ground
- Cell need not be the same horizontal width
- Other design rules must be met as well



Two cells, abutted

Cell Placement in Two Adjacent Rows



- Each row may be flipped vertically
- VDD and ground rails of each row may be abutted
- Some cells may overlap
- Overlap of select and substrate contact actives must be allowed

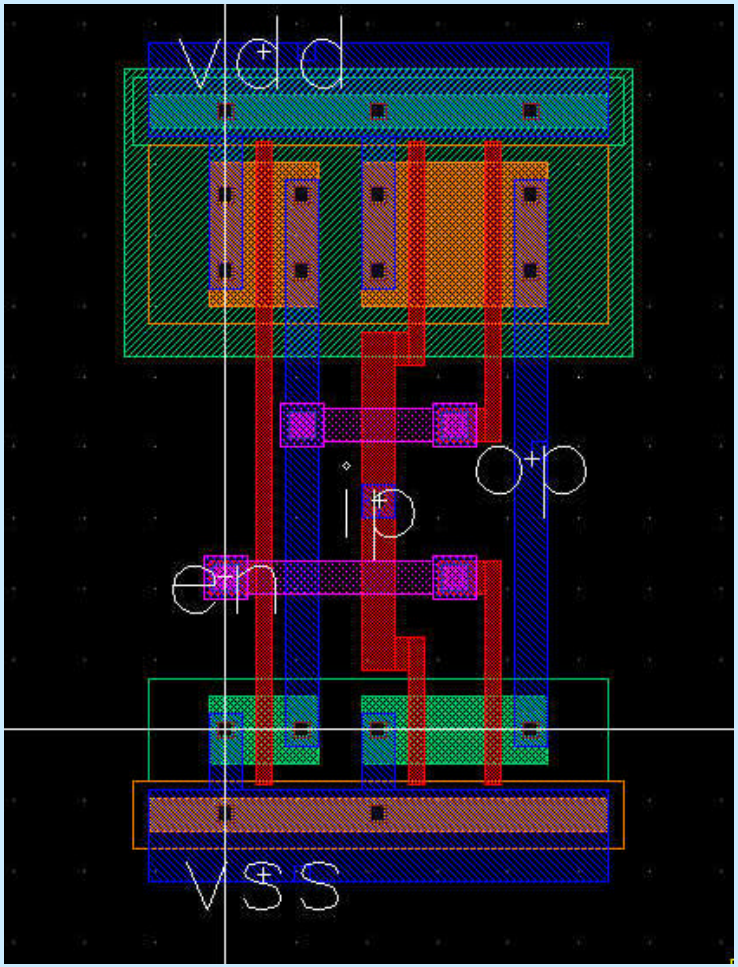
Choice on Directions of Metal Tracks

- **Definition: Preferred direction = default metal tracks directions for the PNR tools**
  - **Decided by layout library designer**
  - **A common convention is HVH (horizontal-vertical-horizontal): horizontal metal1, vertical metal2, horizontal metal3, etc.**
  - **However, the PNR tool may also use nonpreferred directions as it sees fit**
- **Metal tracks inside cells should follow nonpreferred directions**
  - **Thus, if use HVH default, use VHV inside cells**

Guidelines on Intracell Metal Routing

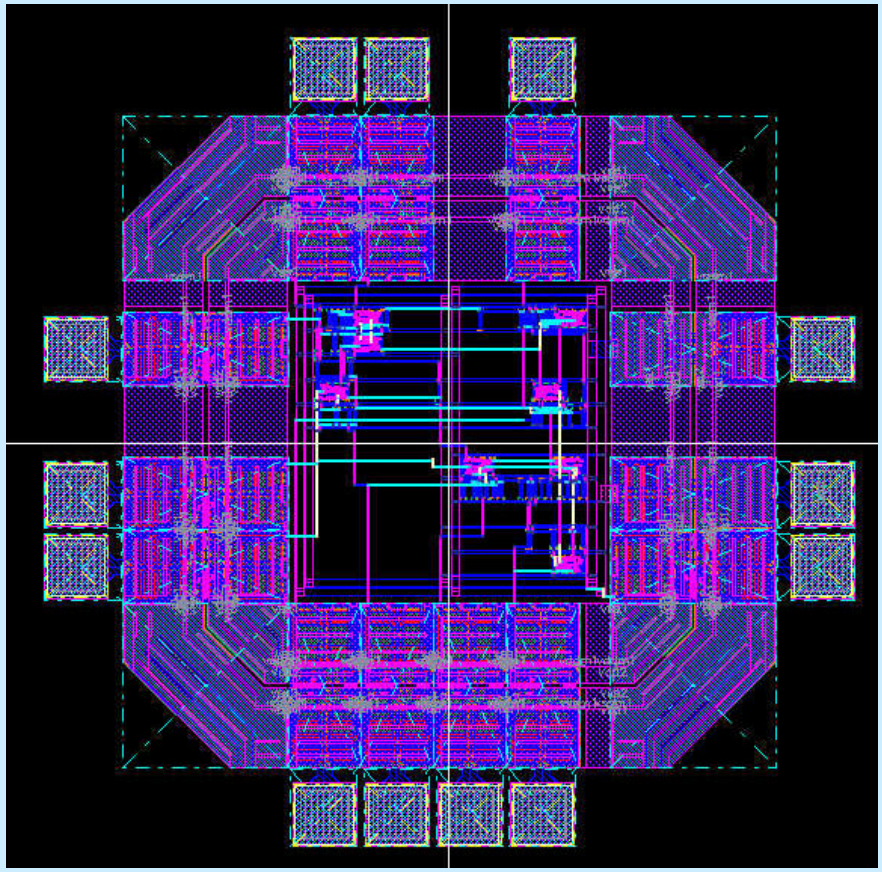
- Not only should the intercell metal layers follow nonpreferred directions, they should use the pitch and grid of the metal above it.
  - For example, if use HVH, with metal2 pitch = 1 μm and metal3 pitch = 2 μm, should align metal2 inside cell horizontally with 2 μm pitch
  - Helps the PNR tool in placing vias
- May not apply to metal1 in complicated cells in, say, five-metal tech
  - No space for metal1 routing over the cell anyway

Example of Cell Constructed

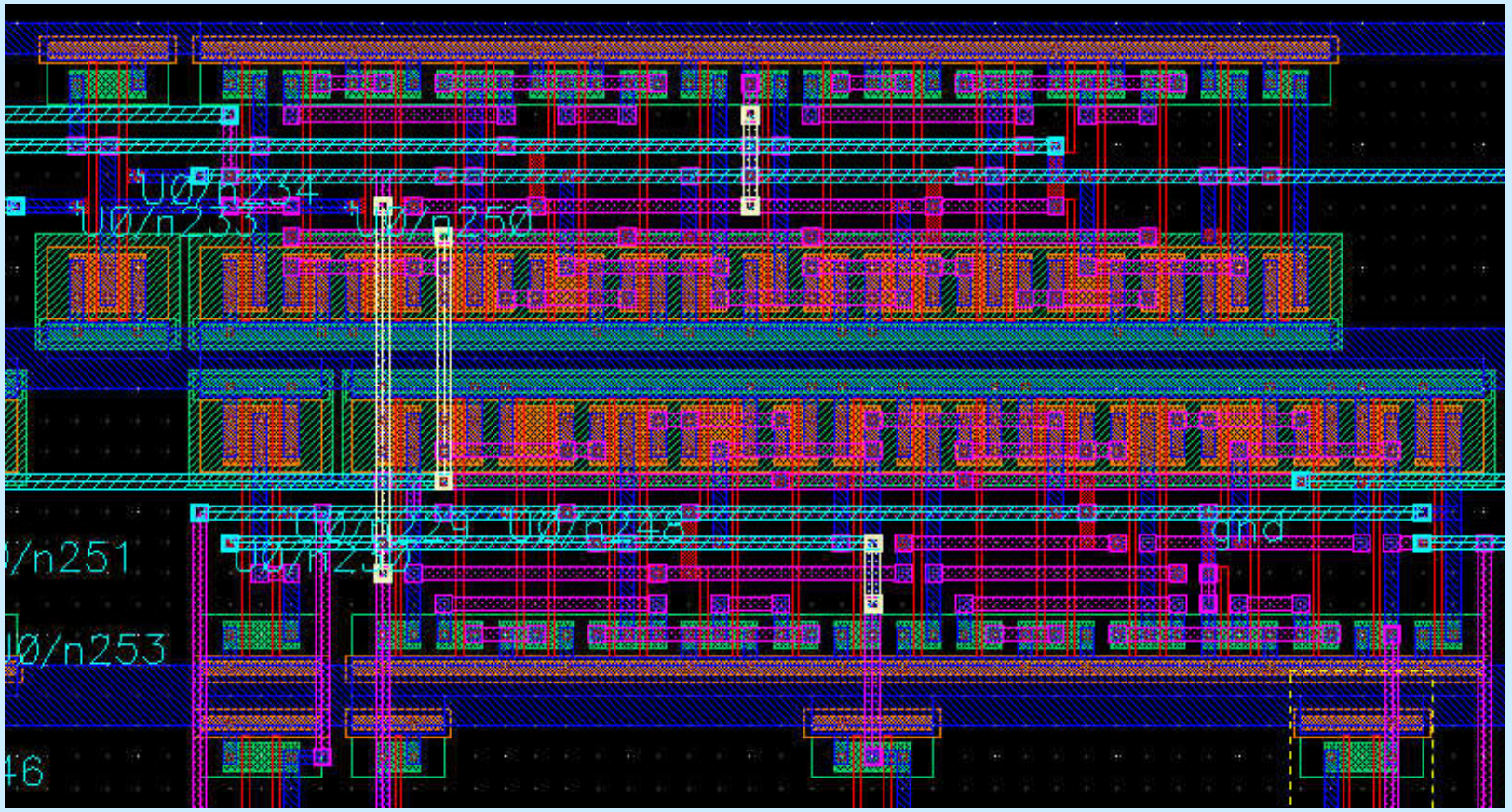


- This tristate inverter uses a 5-metal tech
- Use HVH default here
  - blue = metal1, pink = metal2
- Here metal1 is run vertically, and metal2 horizontally, inside the cell, even though outside the cell, m1 = horizontal, m2 vertical

Example of Placed Circuit



Snapshot of Two Adjacent Rows



metal1/2/3/4 = deep blue / pink / light blue / yellow

If Interested to Know More

- For Cadence PNR tools, can use openbook and open the following file:

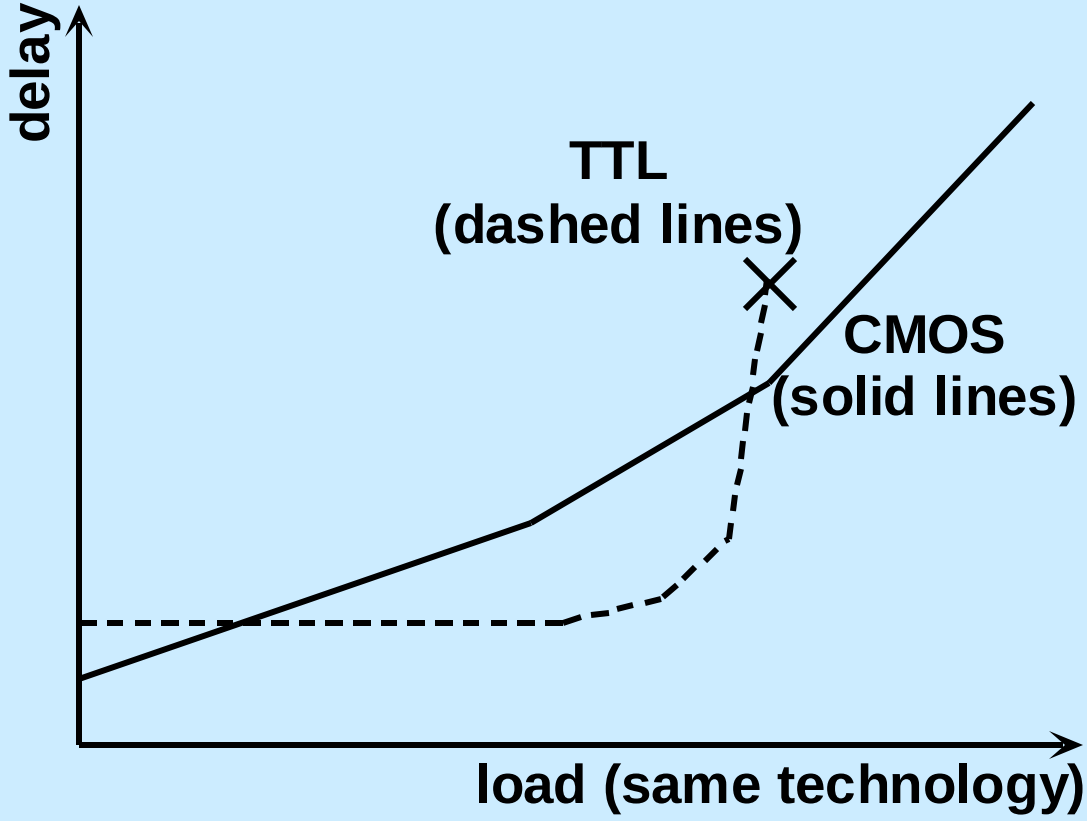
  /software/cadence2000/DSMSE53/doc/abstract/appD.doc (guidelines for cell library design)

- The contents of the aforementioned document may not apply for PNR tools from a different vendor

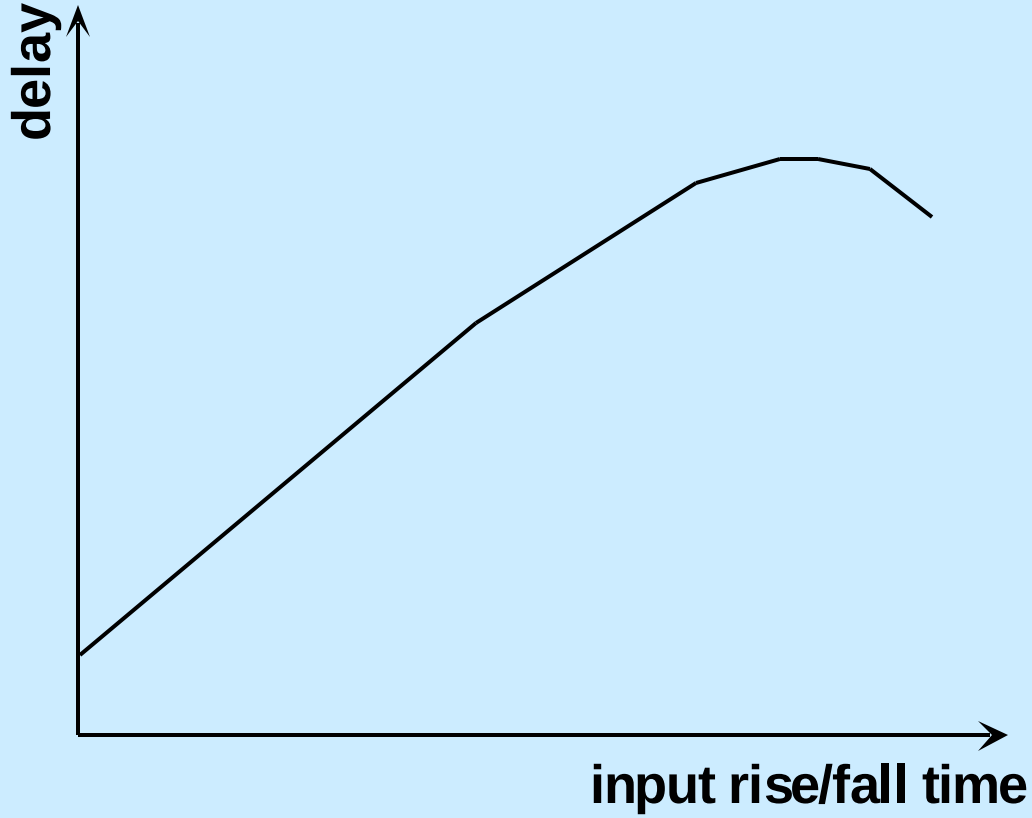
Timing and Power Characterization

- What is the purpose? Modeling vs. Quick Comparison vs. Ballpark Estimate
  - Modeling Needs Many Parameters
  - The resulting model may not be intuitively obvious
  - May be inappropriate for quick comparison
- Needs to understand what SPICE reports
  - SPICE does not report everything important
- Needs to understand how CMOS gates behave
  - Unlike TTL in some ways

CMOS: Load Dependent but No Fanout Limit

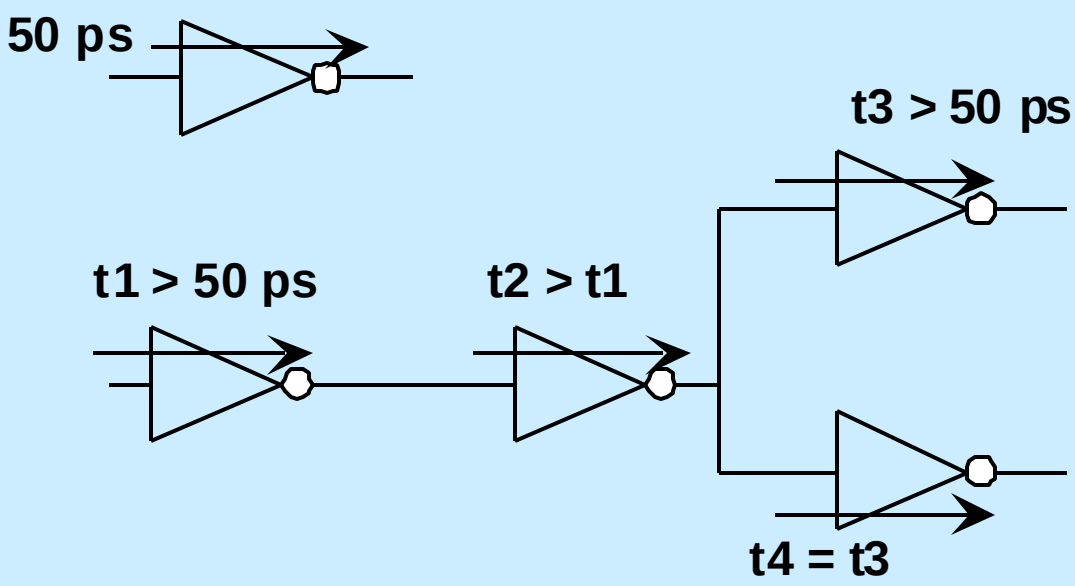


CMOS – Delay also Depends on Input Slope



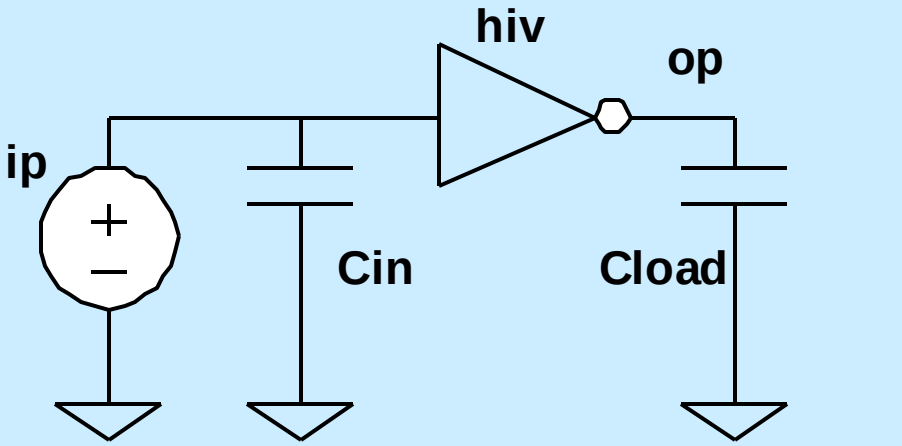
- Dependence should be almost linear
- Hence, longer rise/fall time at input should translate to longer input-to-output delay always
- However, strongly depends on how rise/fall times are defined

What all those come to ...



- Total delay not equal (3 x 50 ps)
- Cannot simply add gate delays as in TTL case
- Still true that delay = t1 + t2 + t3
- Modeling and comparison must quantify this dependence on load / input slope

Caution: SPICE measures only resistive power!



.measure p_av avg p(hiv) from=... to=...

- The measure statement measures only "resistive" power dissipation
  - short circuit power
  - leakage
  - $0.5*CV^2$ due to C_{load}
- Will not measure $0.5*CV^2$ due to C_{in}
- $0.5CV^2$ due to C_{in} also has to be measured for comparisons

Timing and Power Characterization

- Synthesis Tool needs logic model
- Also need to include delay and power dissipation parameters
- Found during Characterization Process
- Many timing models available (e.g. linear, piecewise linear, nonlinear, DCM2)
- At VTVT group, use linear delay model, as it needs fewest simulation in characterization, but plan to use lookup-table based model in the future.

Timing Characterization – linear model

- Parameters to characterize:
  - Intrinsic Delay
  - Slope Sensitivities – quantifying delay dependence on input rise/fall times
  - Output Resistance – quantifying delay dependence on load capacitance
  - Setup time of sequential cells
  - Input/Output Capacitances (used for both power and delay estimation)
- Piecewise linear model has several values for various range of independent variable (load, input rise/fall time) values

Timing Characterization – Nonlinear Model

- Fully lookup-table based
- Synthesis tools perform interpolation based on data on table
- The only model currently supported by Cadence
- Offers the best accuracy
- Requires largest number of simulation to perform

Linear Delay Model Example

- **Synopsys CMOS Cell Delay Model:**
  - **Delay = (Intrinsic Delay) + (Transition Delay) + (Slope Delay)**
- **Linear Relationships:**

Transition Delay = (Output Resistance) ´ (Load Capacitance)

Slope Delay = (Slope Sensitivity) ´ (Input Transition Delay)

Example Linear Delay Calculation

- A cell has intrinsic delay of 80 ps, slope sensitivity of 0.4, and output resistance of 2 kOhms
- It drives a load of 15 fF
- Its input has transition delay of 30 ps
- Hence slope delay = (0.4 ´ 30) = 12 ps, while transition delay is (2 ´ 15) = 30 ps
- Cell delay is 80 + 30 + 12 = 122 ps
- The above value, not intrinsic delay, must be used in critical path estimation

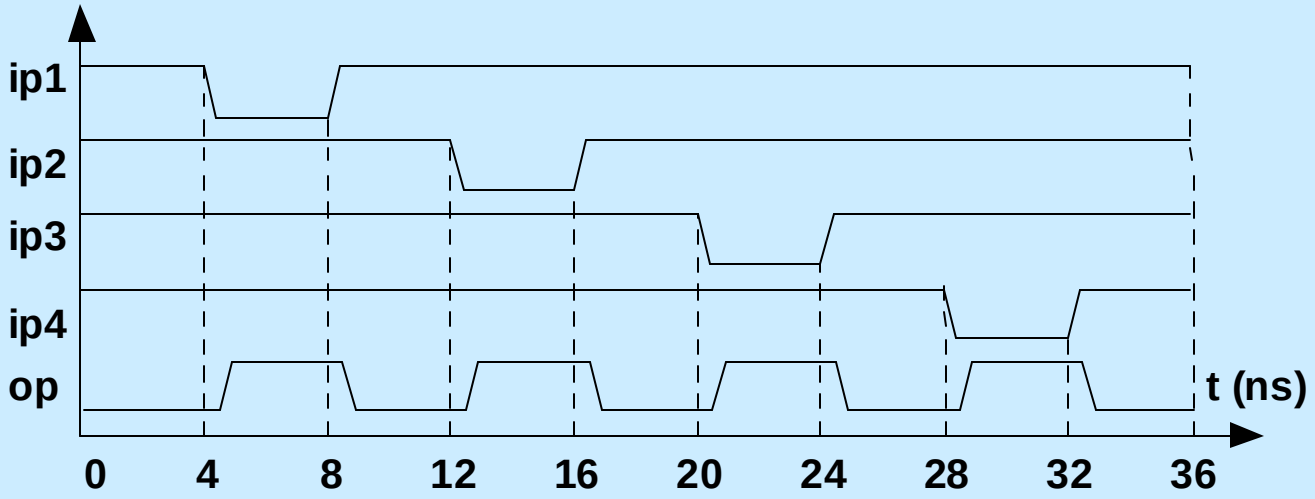
Power Characterization

- Most simulation-based tools estimate energy first, then divide by time to get power
- Typical parameters to characterize:
  - Energy per transition on each pin
  - Leakage power
  - Input/Output Capacitances (but already characterized in timing characterization)

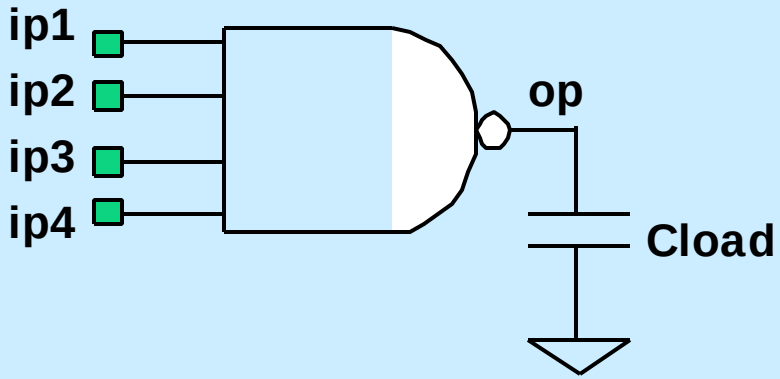
Synopsys Power Model

- Actualy energy, instead of power, is calculated first
- Total Energy = Static Energy + Dynamic Energy
- Average Power = Total Energy / Simulation Time
- Static Energy = S(Static Power´ Dissipation Time)
- Static Power could be equated with leakage for CMOS
- Different values could be given for energies for various conditions of a cell, e.g. static power for output=high and for output=low

Calculation Example



$$\text{Dynamic Power} = [(4 \times E_{rise}(op) + 4 \times E_{fall}(op)) + 8 \times E_{switching}] / 36ns$$



Internal Energy Parameters

- Simple Combinational Cells (AND, NAND), etc
  - For output pins only
  - May depend on load capacitance and input rise/fall times
- Sequential cells, combinational cells with internal loads (muxes, AND-OR-invert, etc), and tristate cells
  - Both input and output pins
  - May depend on load capacitance and input rise/fall times