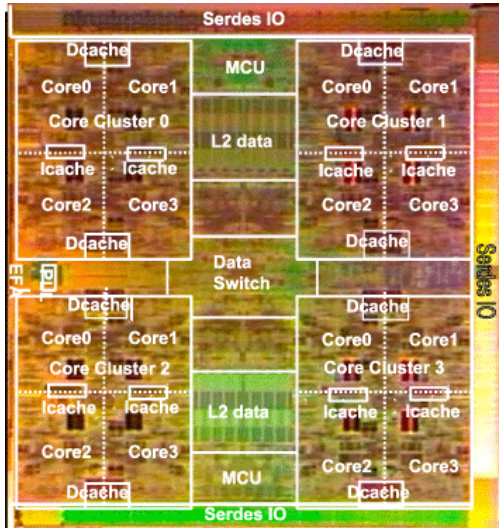
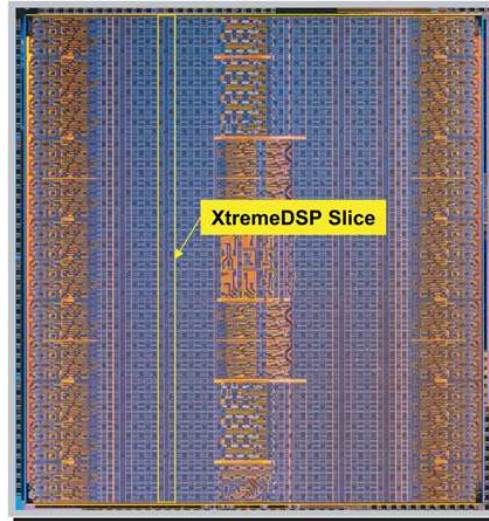


Flavors of Integrated Circuits

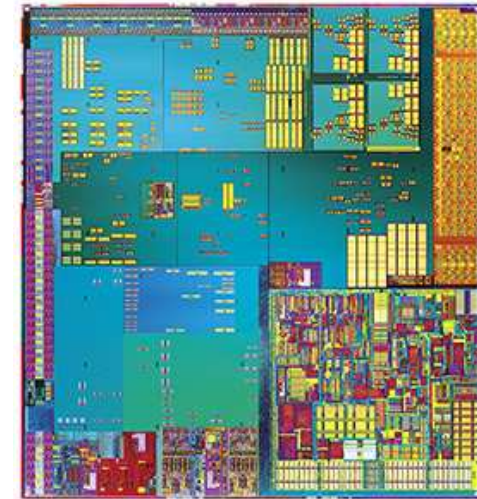
Microprocessor



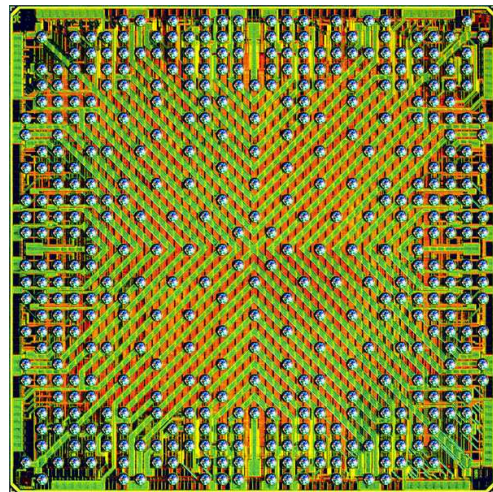
FPGA



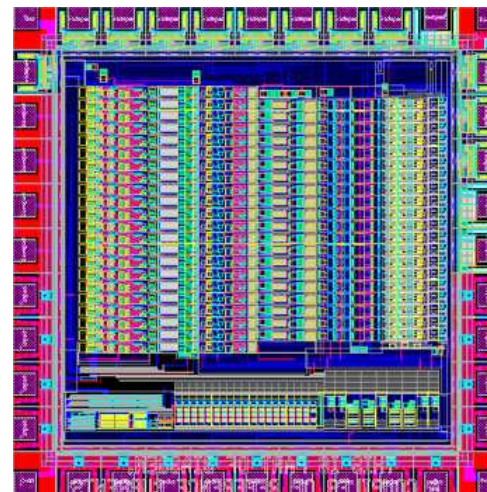
SoC



DSP



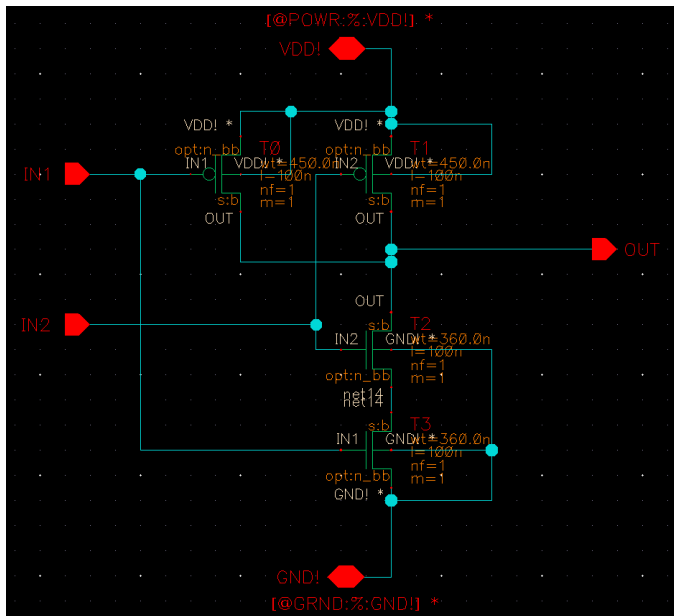
Microcontroller



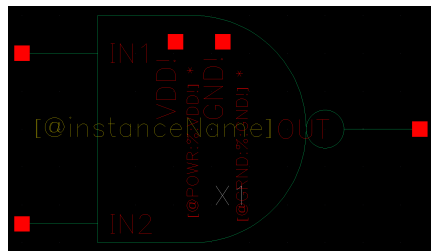
ASIC Design Flow

Designing a chip using a Standard Cell Flow

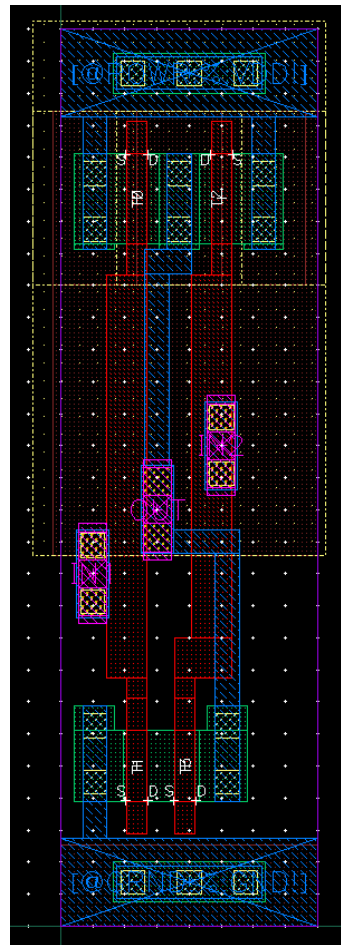
NAND 2X1



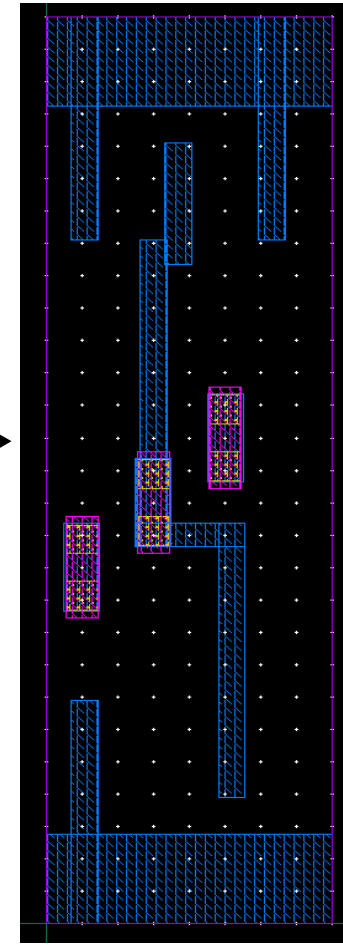
Schematic



Symbol

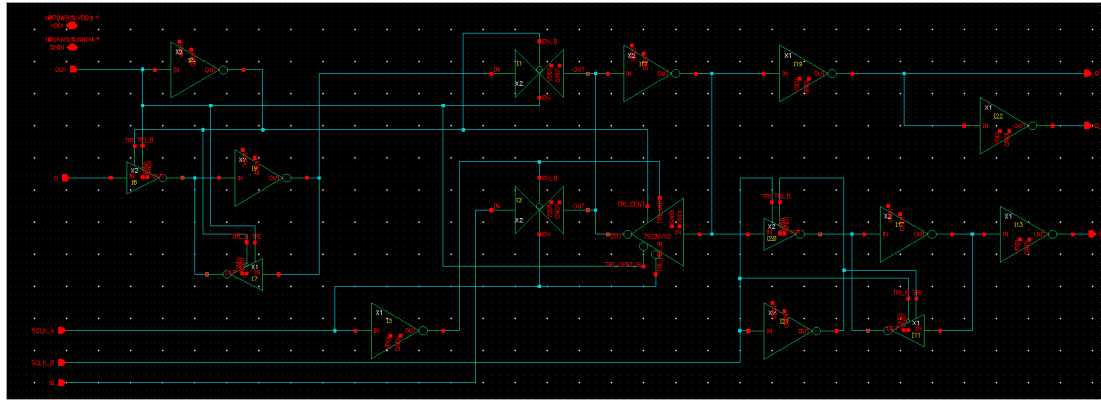


Layout

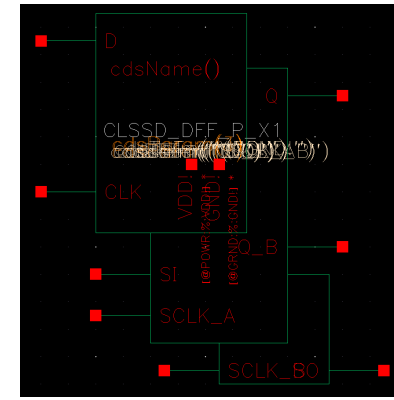


Abstract

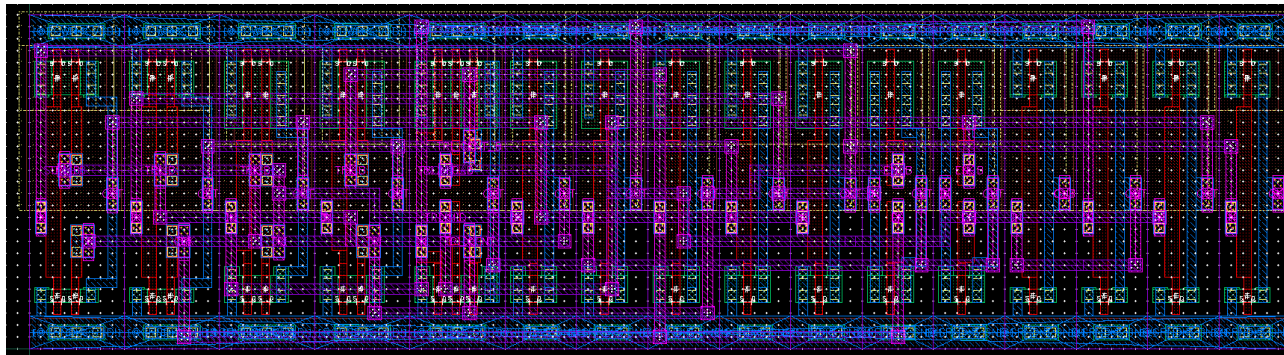
ASIC Design Flow (Clocked LSSD Scan Flop)



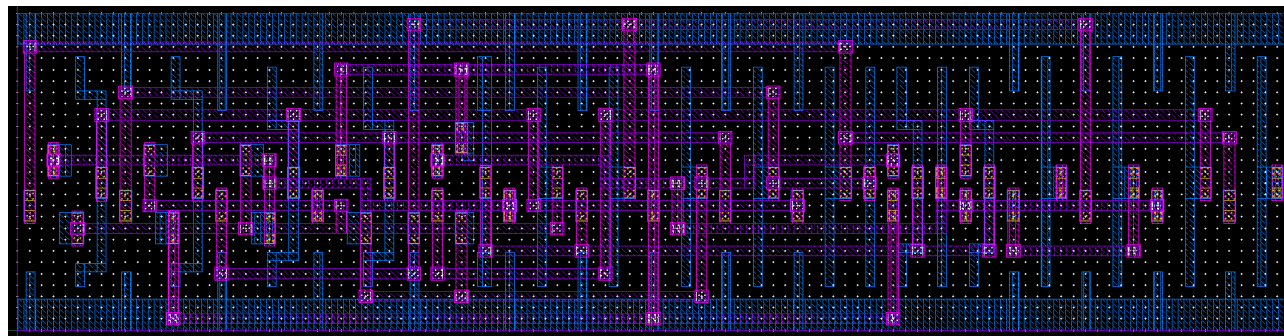
Schematic



Symbol



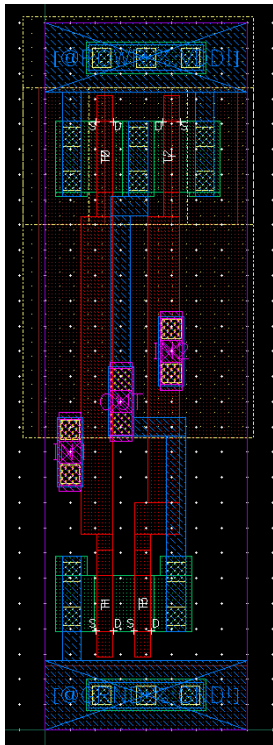
Layout



Abstract

ASIC Design Flow Timing Characterization

Extract RC model



Layout

```

Session Edit View Bookmarks Settings Help
// Library name: MosisNewChipProject
// Cell name: 040224
// View name: calibre
subject: 040224 inh_GND IN1 IN2 OUT inh_PWR
MT2 (MT2_d MT2_g net14 MT2_b) nfet w3.6e-07 l=1e-07 par=1 m=1 \

MT3 (net14 MT3_g MT3_s MT3_b) nfet w3.6e-07 l=1e-07 par=1 m=1 \

MT1 (MT1_d MT1_g MT1_s MT1_b) pfet w4.5e-07 l=1e-07 par=1 m=1 \

MT0 (MT0_d MT0_g MT0_s MT0_b) pfet w4.5e-07 l=1e-07 par=1 m=1 \

VDD0_19 (MT0_b MT1_b) resistor r=0.01
VDD0_18 (MT0_b D4 noref_pos) resistor r=0.01
VDD0_17 (VDD0_2 VDD0_1) resistor r=0.100594
VDD0_16 (VDD0_24 VDD0_1) resistor r=0.0387341
VDD0_15 (VDD0_20 VDD0_2) resistor r=0.809667
VDD0_14 (VDD0_4 VDD0_3) resistor r=0.100594
VDD0_13 (VDD0_27 VDD0_3) resistor r=0.00893864
VDD0_12 (VDD0_22 VDD0_4) resistor r=0.809667
VDD0_11 (VDD0_24 MT0_b) resistor r=10
VDD0_10 (VDD0_27 MT0_b) resistor r=10
VDD0_9 (VDD0_20 MT0_s) resistor r=7.5
VDD0_8 (VDD0_22 MT1_s) resistor r=7.5
VDD0_7 (inh_PWR VDD0_24) resistor r=0.0834273
VDD0_6 (VDD0_27 inh_PWR) resistor r=0.0834273
ROUT_27 (MT0_d MT1_d) resistor r=0.01
ROUT_26 (OUT_2 OUT_1) resistor r=0.23415
ROUT_25 (OUT_15 OUT_1) resistor r=0.0196693
ROUT_24 (OUT_3 OUT_2) resistor r=0.8033932
ROUT_23 (OUT_4 OUT_3) resistor r=1.388
ROUT_22 (OUT_7 OUT_4) resistor r=0.80784746
ROUT_21 (OUT_6 OUT_5) resistor r=0.383625
ROUT_20 (OUT_12 OUT_5) resistor r=0.8678475
ROUT_19 (OUT_15 OUT_6) resistor r=0.8491733
ROUT_18 (OUT_9 OUT_7) resistor r=0.159042
ROUT_17 (OUT_10 OUT_9) resistor r=0.80784746
ROUT_16 (OUT_29 OUT_10) resistor r=0.144583

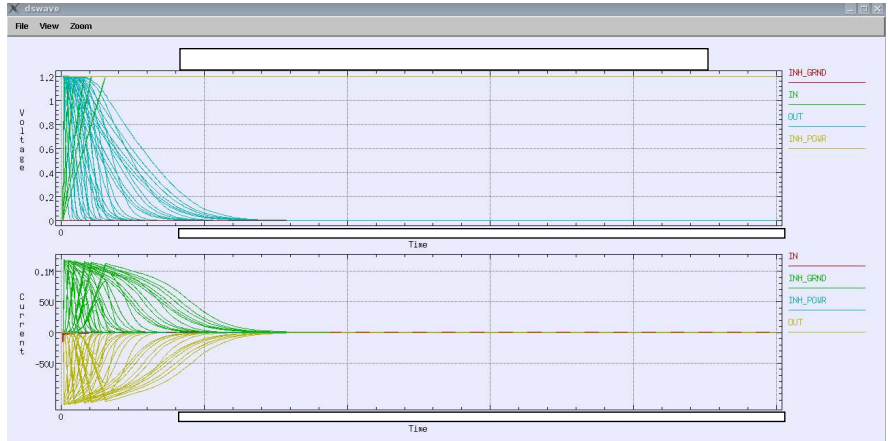
```

Automatic timing characterization through spice simulation runs

```

Session Edit View Bookmarks Settings Help
+-----+-----+
+ Design : 040224 +
+-----+-----+
cell: 040224 {
cell_footprint: nand2;
area: 5.7344;
cell_leakage_power: 0.001951;
rail_connection: INH_GND, RAIL_INH_GND;
rail_connection: INH_PWR, RAIL_INH_PWR;
pin(IN1) {
direction: input;
input_signal_level: RAIL_INH_PWR;
capacitance: 0.00235293;
rise_capacitance: 0.00235293;
fall_capacitance: 0.00233986;
rise_capacitance_range ( 0.00235286, 0.00254153 );
fall_capacitance_range ( 0.00233963, 0.0025395 );
ecsm_capacitance(rise) {
index_1: "0.08, 0.32, 0.64, 1.2, 1.6, 2.4";
values: ;
}
ecsm_capacitance(fall) {
index_1: "0.08, 0.32, 0.64, 1.2, 1.6, 2.4";
values: ;
}
max_transition: 2.4;
internal_power() {
rise_power(passive_energy_template_6x1) {
index_1 ("0.08, 0.32, 0.64, 1.2, 1.6, 2.4");
values: ;
}
ecsm_power(passive_energy_template_6x1) {
ecsm_power_type: rise;
index_1 ("0.08, 0.32, 0.64, 1.2, 1.6, 2.4");
ecsm_current_wavform "0", "INH_GND" {
index_1: "0, 0.00241764, 0.00208302, 0.00229687, 0.00205356, 0.00311001, 0.0013066, 0.0020692, 0.00467592, 0.00528148, 0.00460656, 0.00533302, 0.0046686, 0.00538005, 0";
values: ;
}
ecsm_current_wavform "1", "INH_GND" {
index_1: "0, 0.00055946, 0.000524895, 0.000545635, 0.000529081, 0.000593198, 0.000668007, 0.00078764, 0.00228995, 0.00232638, 0.00138789, 0.001157, 0.00115794, 0.00119958, 0.00119174, 0.00124966, 0.00124444, 0";
values: ;
}
ecsm_current_wavform "2", "INH_GND" {
index_1: "0, 0.00277049, 0.0002556, 0.000269614, 0.00026889, 0.000288596, 0.000331454, 0.000466001, 0.00108583, 0.00106163, 0.000590653, 0.000556119, 0.000549, 0.000586701, 0.000571637, 0.000626882, 0.000608097, 0.00064497, 0";
values: ;
}
ecsm_current_wavform "3", "INH_GND" {

```



Timing characterization file (synopsys lib format)

ASIC Design Flow

```

-- Company:
-- Engineer: Jim Plusquellic
--
-- Create Date: 16:04:58 01/25/2011
-- Design Name:
-- Module Name: CNTER_BBIT_CLSSD_SCAN
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
-----
Library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.all;

entity CNTER_BBIT_CLSSD_SCAN is
  port(
    CNT_EN, CLK: in std_logic;
    CNT_OUT : out std_logic_vector (7 downto 0)
  );
end entity;

architecture beh of CNTER_BBIT_CLSSD_SCAN is
  signal cnter_reg, cnter_next: unsigned(7 downto 0);
  begin

  process(CLK)
  begin
    if (CLK'event AND CLK = '1') then
      cnter_reg <= cnter_next;
    end if;
  end process;

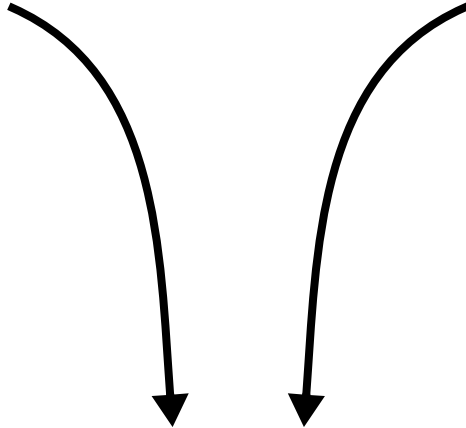
  with CNT_EN select
    cnter_next <= cnter_reg + 1 when '1',
    cnter_reg when others;

  CNT_OUT <= std_logic_vector(cnter_reg);
end beh;

```

Behavioral VHDL code

Behavioral Synthesis



```

Session Edit View Bookmarks Settings Help
# INITIALIZE
# Different flows covered in doc, section "Encounter RTL Compiler Synthesis Flows"
# set attribute hdl_search_path /vhdl/
set_attribute hdl_vhdl_read_version 1993
set_attribute hdl_vhdl_case original

#set attribute map_to_master_slave_issd true /

# Information level -- set from 0 (lowest) to 9 (highest)
set_attribute information_level 9

set_attribute lib_search_path /home/jimp/cadence_IBM_9rt/ELC/
set_attribute library std_cells.lib /

find CLSSD_DFF_P_X1/O -libarc +

#set attribute preserve false CLSSD_DFF_P_X1
#set attribute avoid false CLSSD_DFF_P_X1
get_attribute preserve CLSSD_DFF_P_X1
get_attribute avoid CLSSD_DFF_P_X1

# Report other possible problems with scan cells.
filter avoid true [find /libraries -libcell *]
filter preserve true [find /des* -instance *]

# Two modes to synthesize a design: interconnect mode and ple (which uses LEF for better closure
# with back-end tools).
#set attribute lef_library (cns9flp.lef std_cells.lef)

#set attribute cap_table_file cap_file

# DFM -- requires a coefficients file
#read_dfm file.dfm

# READ DESIGN
# =====
read_hdl -vhdl (CNTER_BBIT_SCAN.vhd)

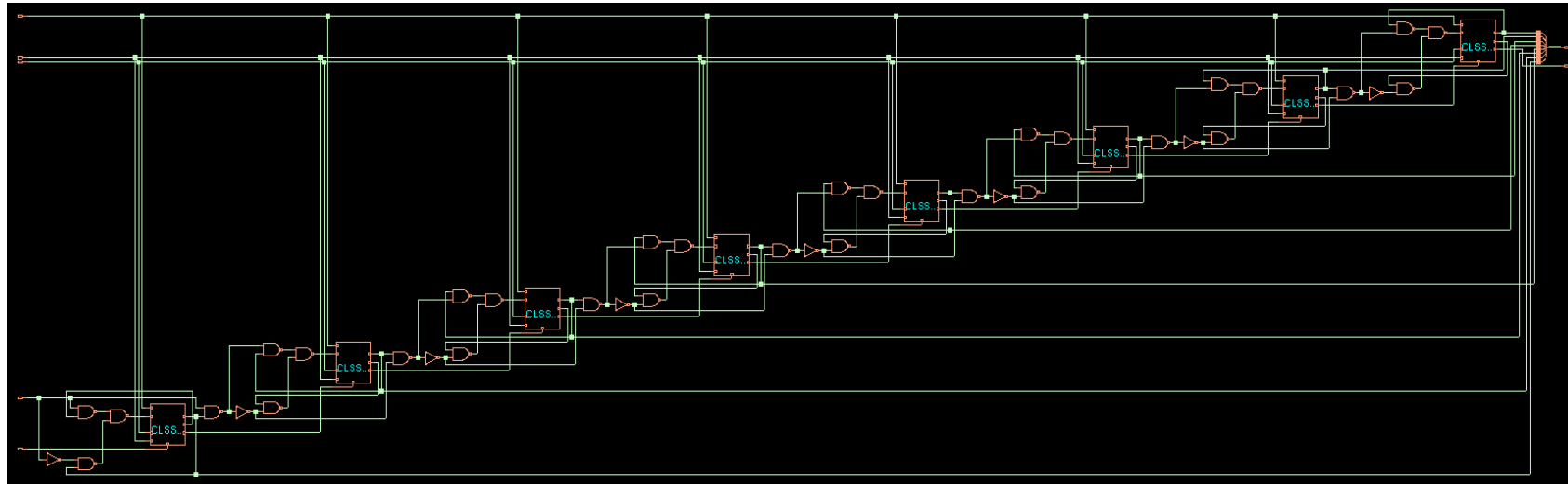
# To allow tracking of any DFT violations (identified later in the flow by the RC-DFT engine) to the
# RTL file name and line number at which the violation occurred, set the following root attribute:
set_att hdl_track_filename_row_col true /

# ELABORATE
# =====
# Builds data structures, infers registers, performs opt (dead code removal) checks semantics
elaborate

# APPLY CONSTRAINTS
# =====
# Constraints include operating conditions, clk wfas and I/O timing
# -- read in SDC constraints. TO use SDC commands from within rc, prefix with dc::
# Use dc::set_time_unit -picoseconds and dc::set_load_unit -femptofarads to set default units --
# ns and pf are default -- however, rc assumes ps and ff

```

RC TCL script



ASIC Design Flow

Final Layout

