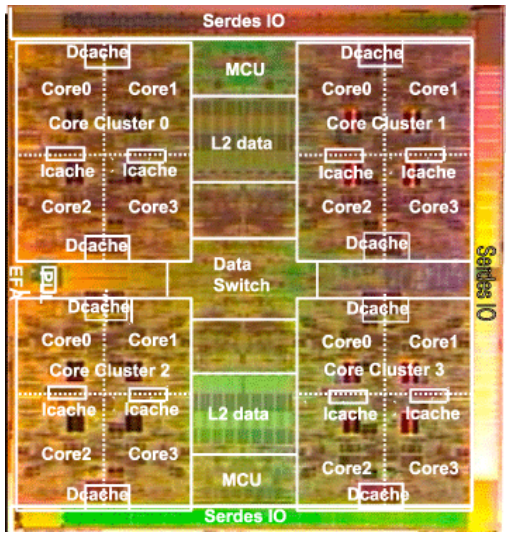
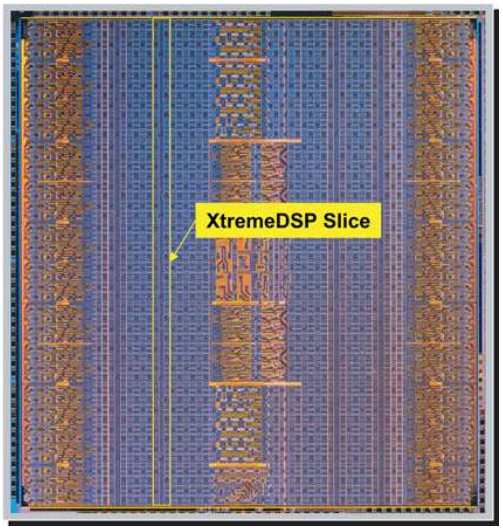
Flavors of Integrated Circuits

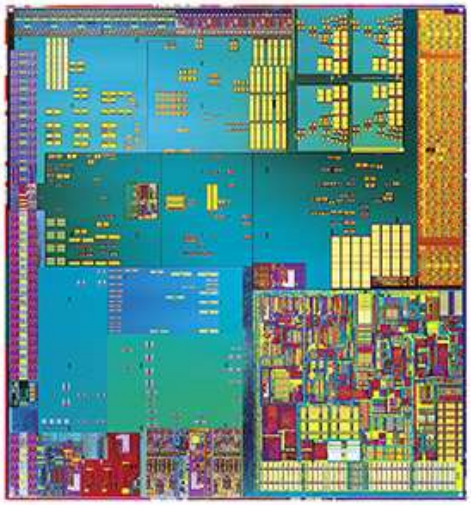
Microprocessor



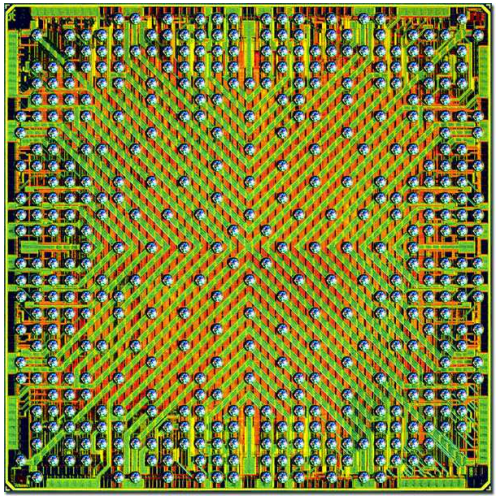
FPGA



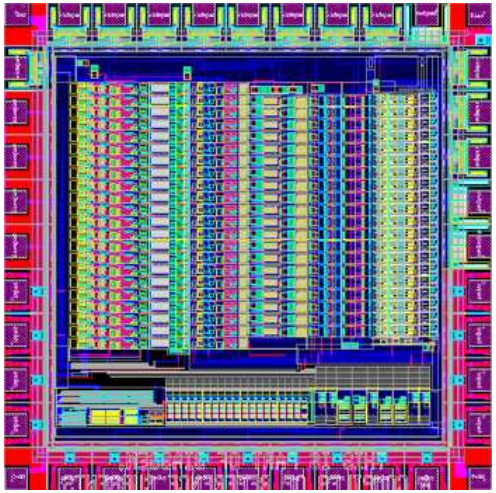
SoC



DSP



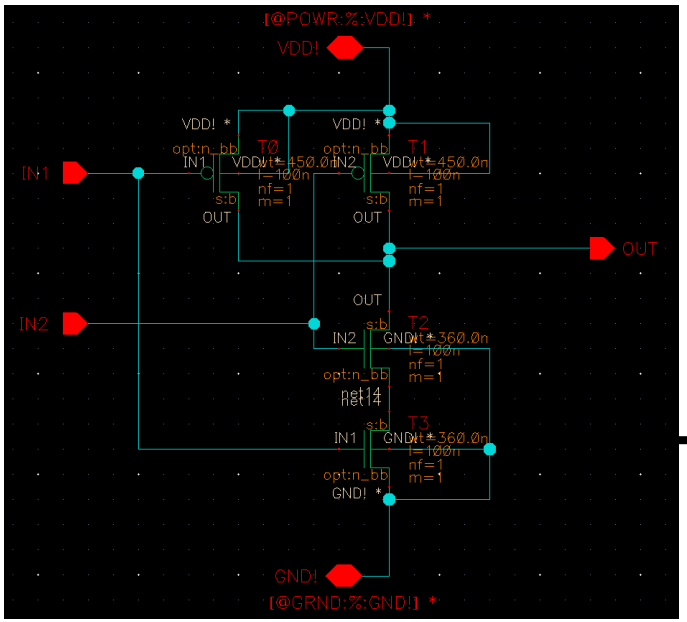
Microcontroller



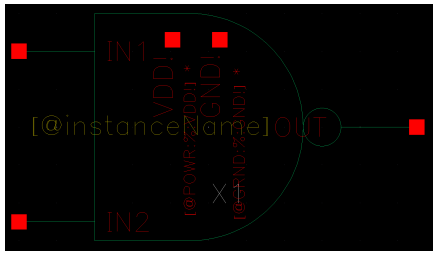
ASIC Design Flow

Designing a chip using a Standard Cell Flow

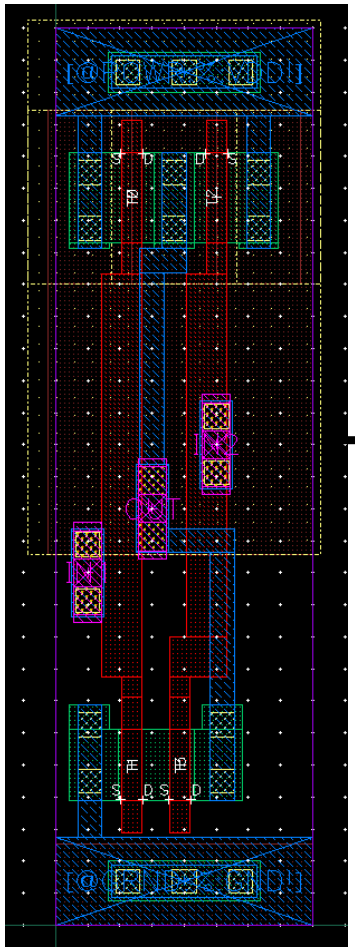
NAND 2X1



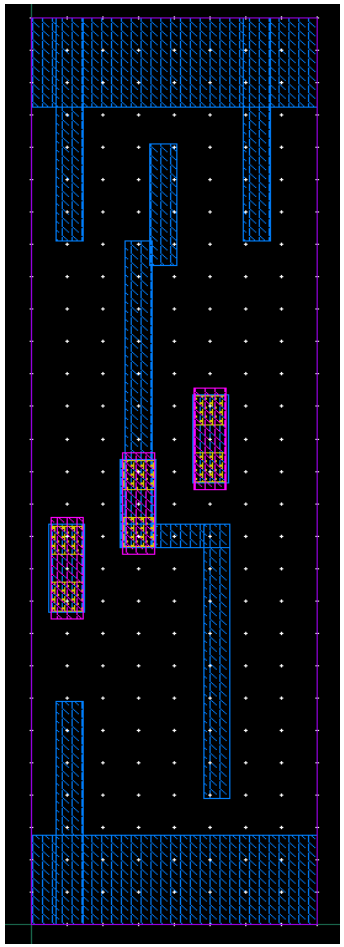
Schematic



Symbol

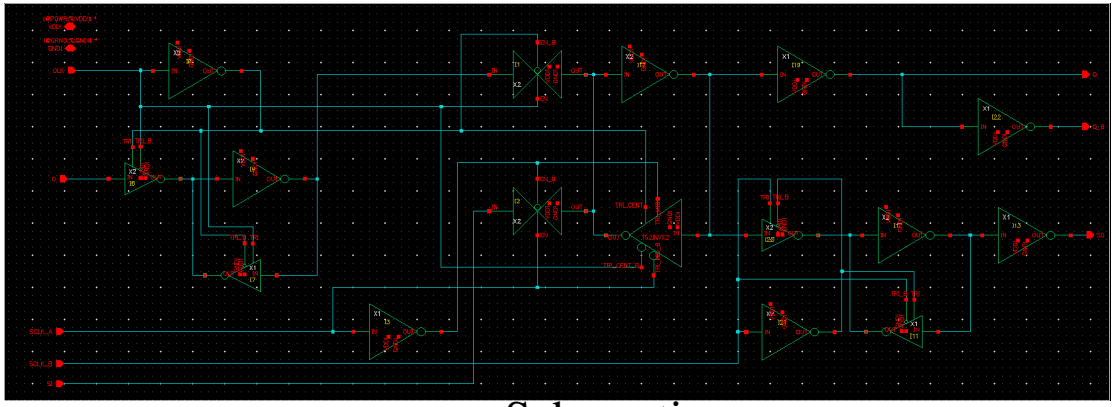


Layout

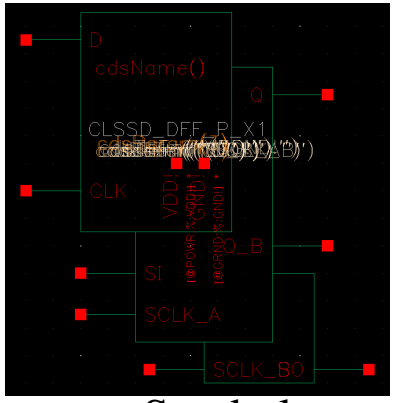


Abstract

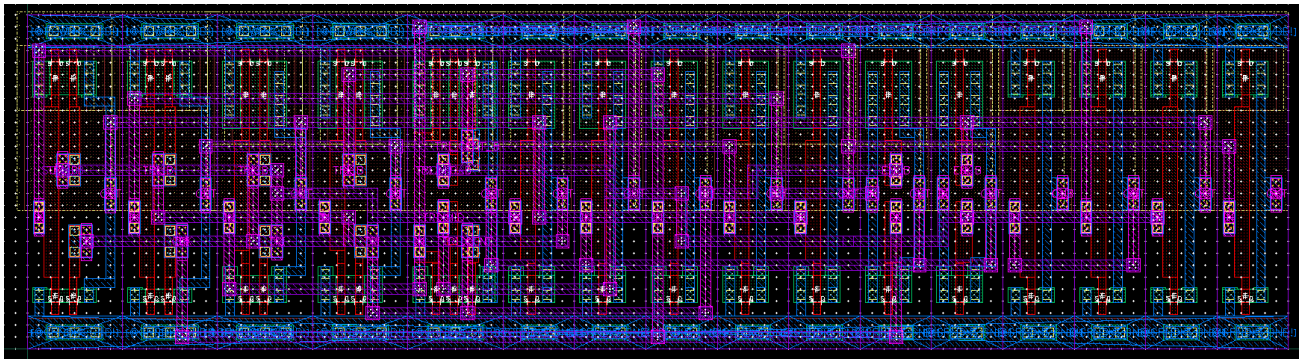
ASIC Design Flow (Clocked LSSD Scan Flop)



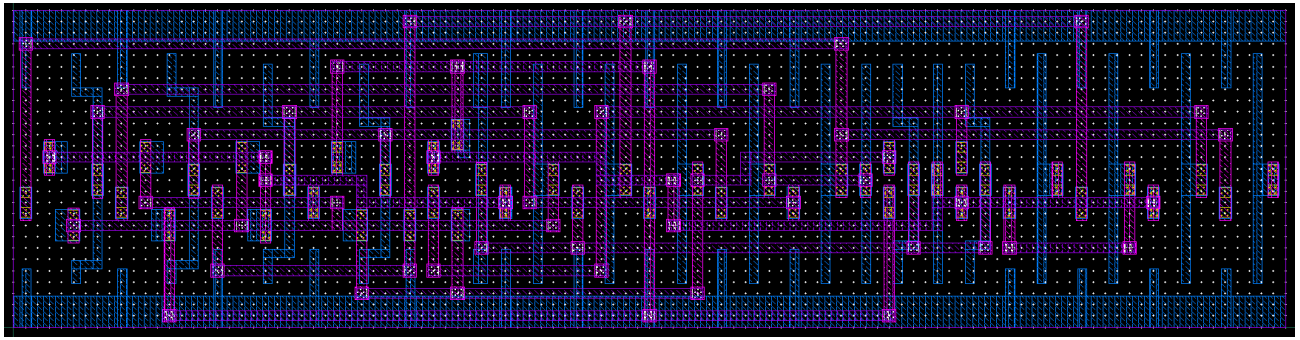
Schematic



Symbol



Layout

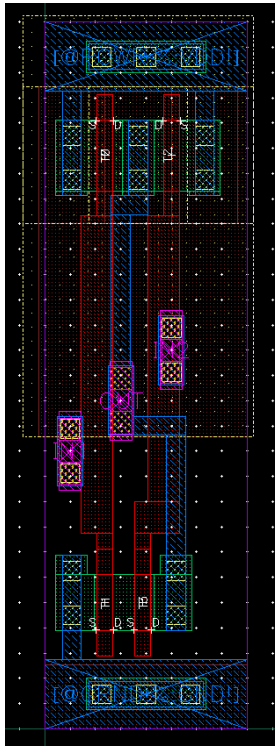


Abstract

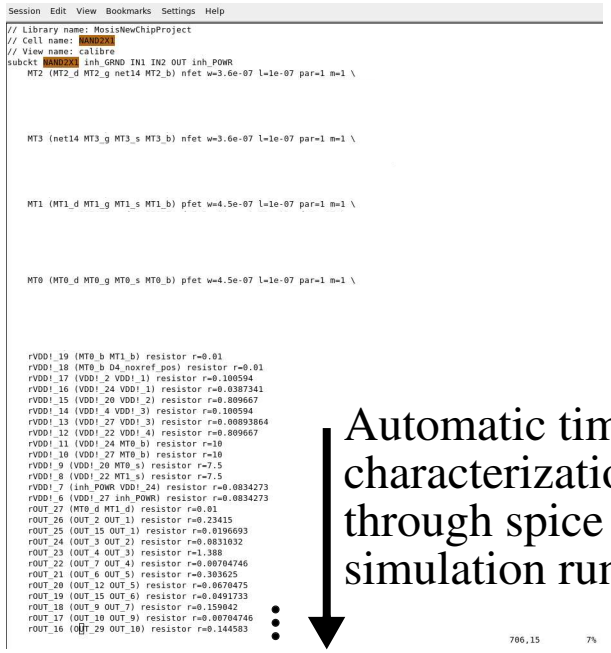
ASIC Design Flow

Timing Characterization

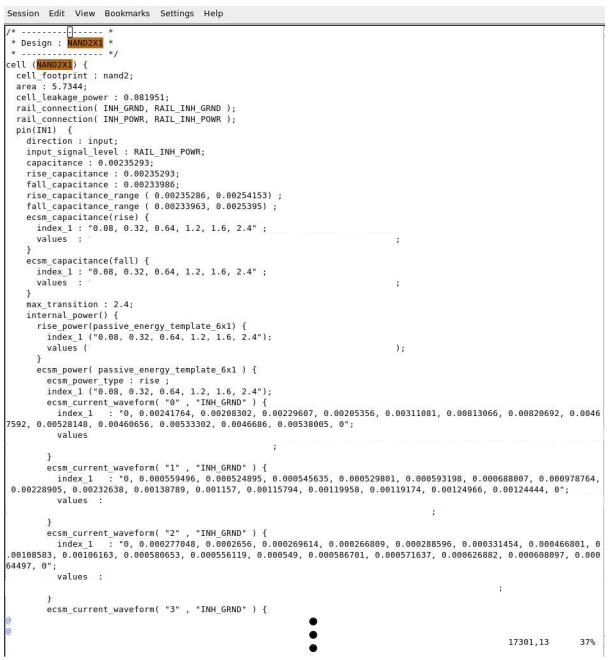
Extract RC model

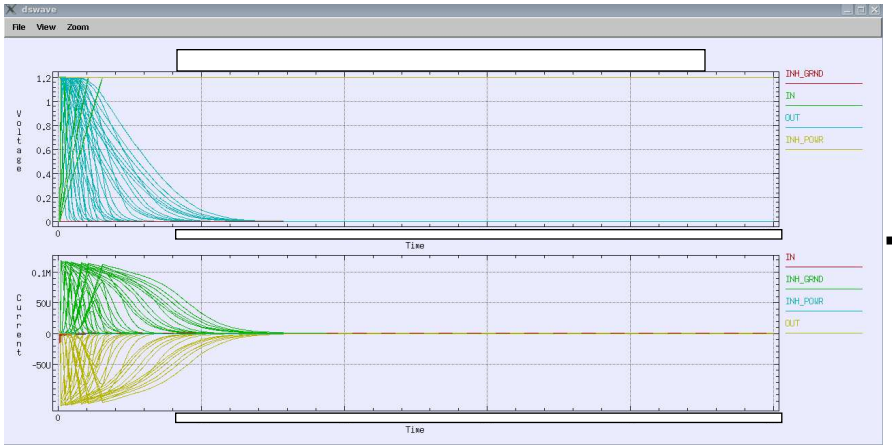


Layout



Automatic timing characterization through spice simulation runs





Timing characterization file (synopsys lib format)

ASIC Design Flow

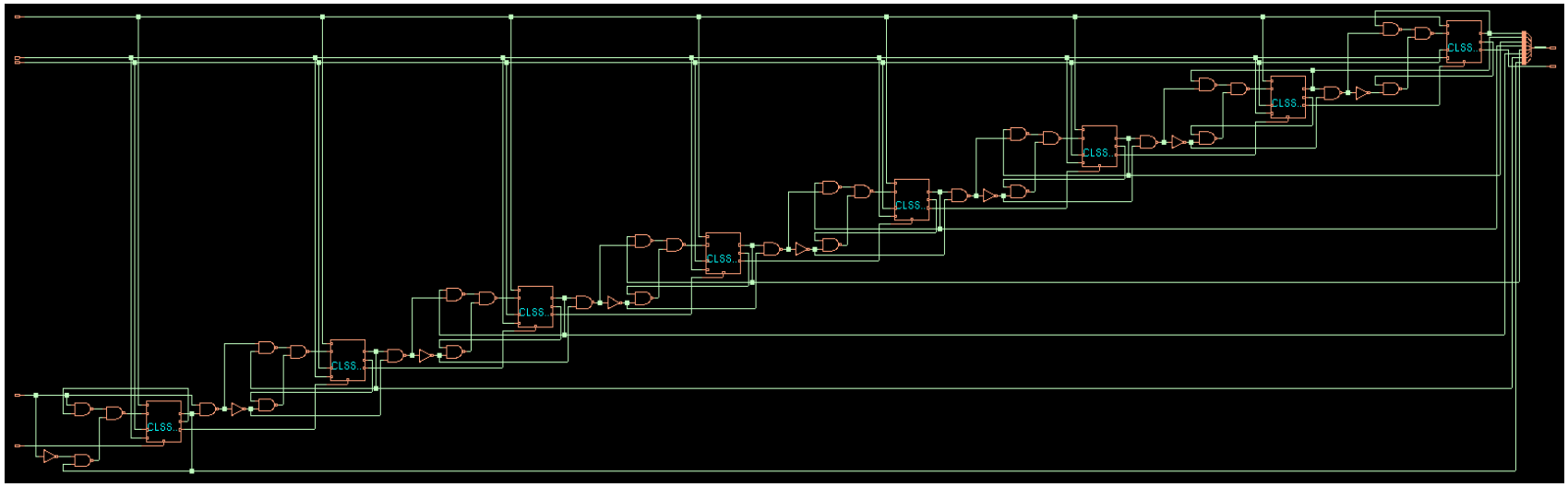
Behavioral Synthesis

Behavioral VHDL code

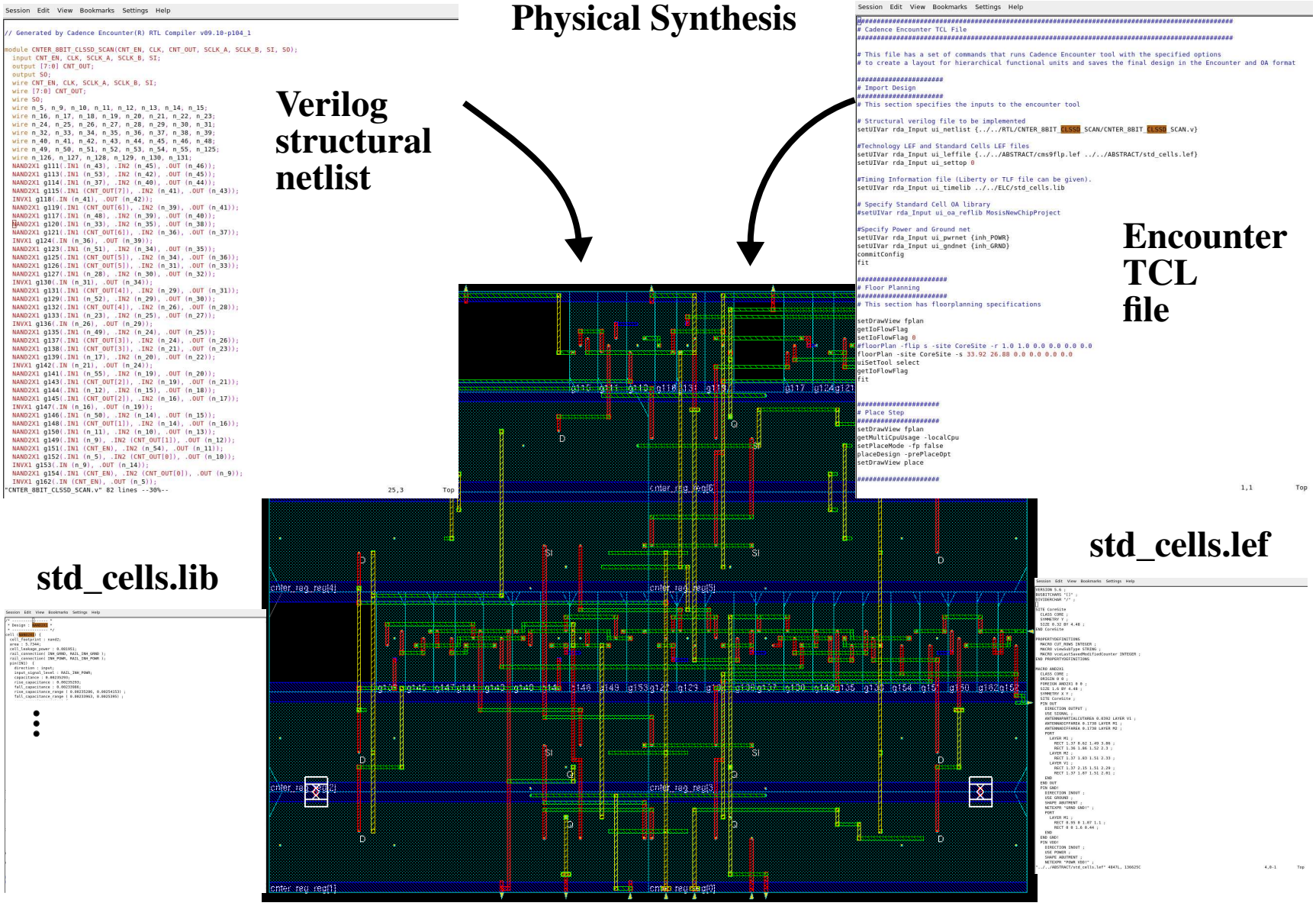
```
----------------------------------------------------------------------------------
-- Company:
-- Engineer: Jim Plusquellic
--
-- Create Date:    16:04:58 01/25/2011
-- Design Name:
-- Module Name:    CNTER_8BIT_CLSSD_SCAN
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.all;

entity CNTER_8BIT_CLSSD_SCAN is
    port(
        CNT_EN, CLK: in std_logic;
        CNT_OUT : out std_logic_vector (7 downto 0)
    );
end entity;

architecture beh of CNTER_8BIT_CLSSD_SCAN is

    signal cnter_reg, cnter_next: unsigned(7 downto 0);
    begin

    process(CLK)
        begin
        if ( CLK'event AND CLK = '1') then
            cnter_reg <= cnter_next;
        end if;
    end process;

    with CNT_EN select
        cnter_next <= cnter_reg + 1 when '1',
                      cnter_reg when others;

    CNT_OUT <= std_logic_vector(cnter_reg);
end beh;
~
~
~
~
~
~
~
"CNTER_8BIT_CLSSD_SCAN.vhd" 48L, 1104C                    26,7          All
```

RC TCL script

```
Session  Edit  View  Bookmarks  Settings  Help
# INITIALIZE
# ============================================================================================
# Different flows covered in doc, section 'Encounter RTL Compiler Synthesis Flows'
# set_attribute hdl_search_path ./vhdl/
set_attribute hdl_vhdl_environment common
set_attribute hdl_vhdl_read_version 1993
set_attribute hdl_vhdl_case original

#set_attribute map_to_master_slave_lssd true /

# Information level -- set from 0 (lowest) to 9 (highest)
set_attribute information_level 9

set_attribute lib_search_path /home/jimp/cadence_IBM_9rf/ELC/
set_attribute library std_cells.lib /

find CLSSD_DFF_P_X1/Q -libarc *

#set_attribute preserve false CLSSD_DFF_P_X1
#set_attribute avoid false CLSSD_DFF_P_X1
get_attribute preserve CLSSD_DFF_P_X1
get_attribute avoid CLSSD_DFF_P_X1

# Report other possible problems with scan cells.
filter avoid true [find /libraries -libcell *]
filter preserve true [find /des* -instance *]

# Two modes to synthesize a design: interconnect mode and ple (which uses LEF for better closure
# with back-end tools).
#set_attribute lef_library {cms9flp.lef std_cells.lef}

#set_attribute cap_table_file cap_file

# DFM -- requires a coefficients file
#read_dfm file.dfm

# READ DESIGN
# ============================================================================================
read_hdl -vhdl {CNTER_8BIT_SCAN.vhd}

# To allow tracking of any DFT violations (identified later in the flow by the RC-DFT engine) to the
# RTL file name and line number at which the violation occurred, set the following root attribute:

set_att hdl_track_filename_row_col true /

# ELABORATE
# ============================================================================================
# Builds data structures, infers registers, performs opt (dead code removeal) checks semantics
elaborate

# APPLY CONSTRAINTS
# ============================================================================================
# Constraints include operating conditions, clk wfms and I/O timing
# -- read in SDC constraints. TO use SDC commands from within rc, prefix with dc::
# Use dc::set_time_unit -picoseconds and dc::set_load_unit -femptofarads to set default units --
# ns and pF are default - however, rc assumes ps and fF
                                                                                1,1           Top
```



ASIC Design Flow



ASIC Design Flow

Final Layout