CMSC 646 Midterm

Name:

This exam is 8 pages long and has 20 questions.

You must show all of your work -- partial credit may be given to partially correct answers, while answers with no justification may not receive full points. Use the back of the exam sheets if you need extra space.

1) (6 pts) Give a one sentence description (for each) that explains why the following VLSI technology trends challenge test.

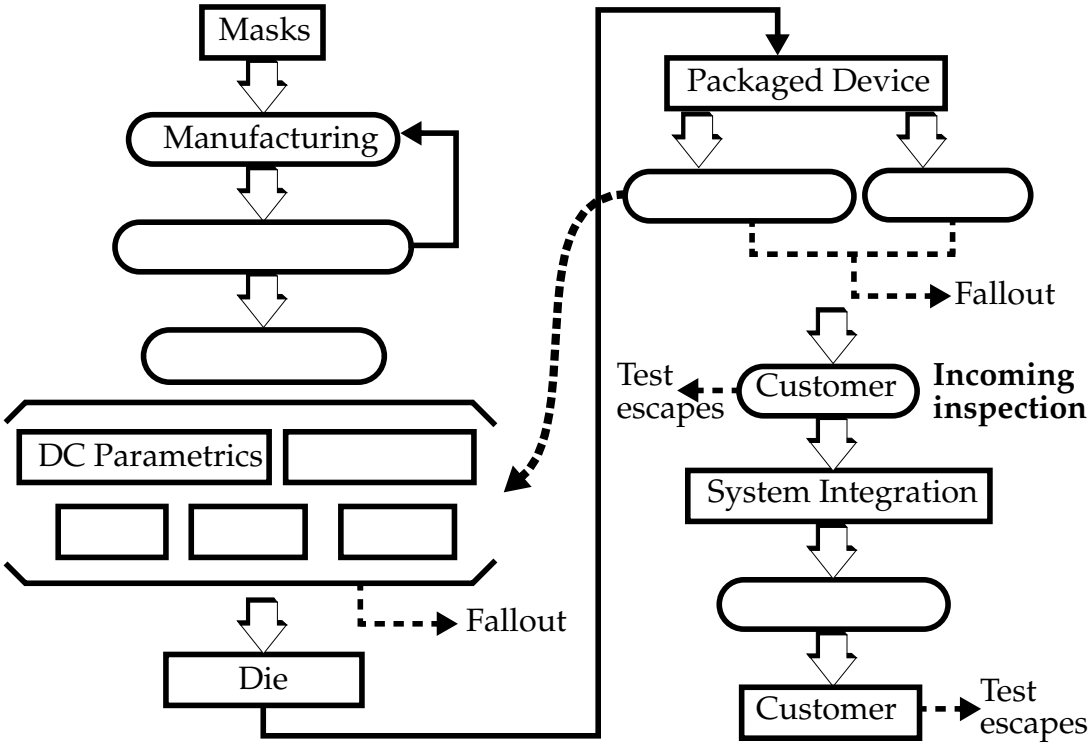
- Rising chip clock rates:

- Increasing transistor density:

2) (4 pts) Briefly distinguish (1 sentence each) between characterization test and production test, i.e., when are they performed in the product's life cycle and for what purpose?

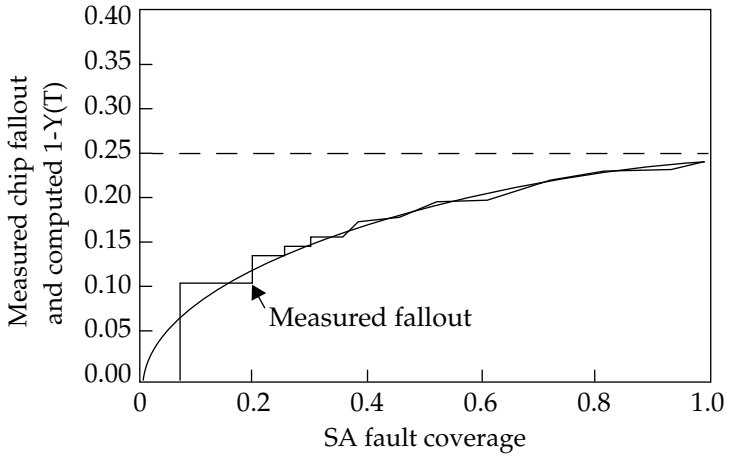
3) (4 pts) Observations indicate that defects are not entirely random, i.e., they are clustered on the wafer. The poisson and negative binomial probability density functions were discussed as models for predicting yield under random and clustering assumptions. Which one is more pessimistic, i.e., predicts lower yields?

4) (8 pts) Fill in the empty blocks in the following test flow diagram.



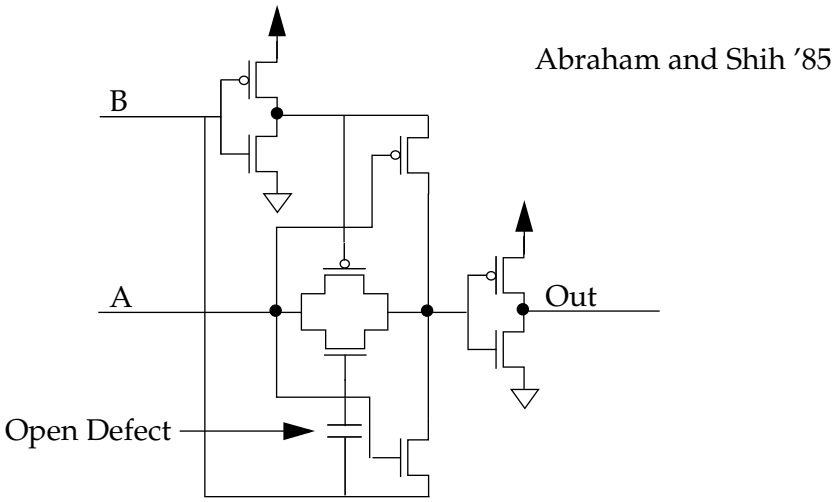
5) (4 pts) Briefly explain why it is difficult to estimate **actual** defect-level (DL)?

6) (6 pts) The following graph can be used to estimate parameters A*f* and β. Once these are known, what else can be estimated?

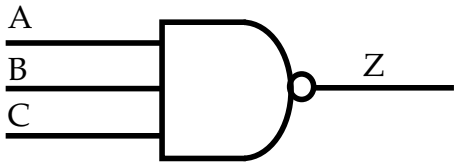


7) (6 pts) The stuck-at fault model assumes all defects cause nodes to behave as if they are shorted to VDD or GND. In CMOS, other possibilities exist with regard to shorting defects. Name them.

8) (4 pts) The following open defect will cause a fault. Name the type of fault it creates and briefly explain why this defect does not result in a stuck-at fault.

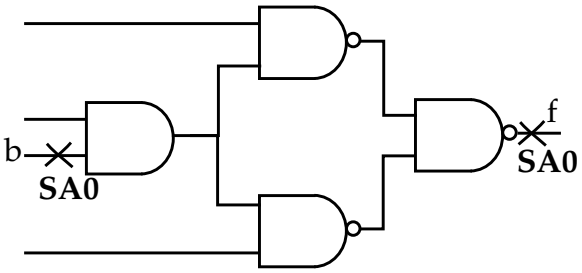


9) (4 pts) Name the faults in the following 3-input NAND gate that are functionally equivalent.

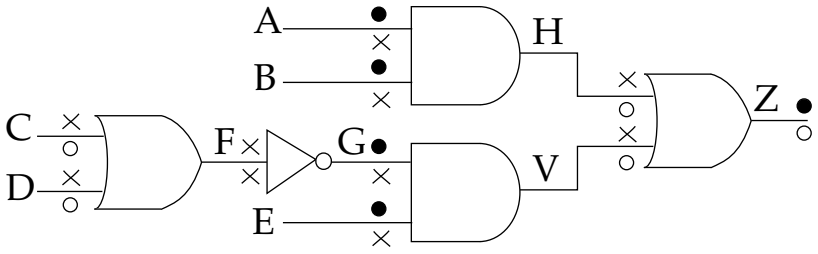


10) (2 pts) Name the dominating fault in the 3-input NAND gate.

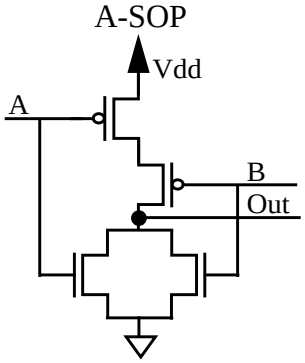
11) (6 pts) Our simple method of fault equivalence collapsing will not determine the faults shown in the figure are functionally equivalent. Briefl yexplain why they are functionally equivalent.



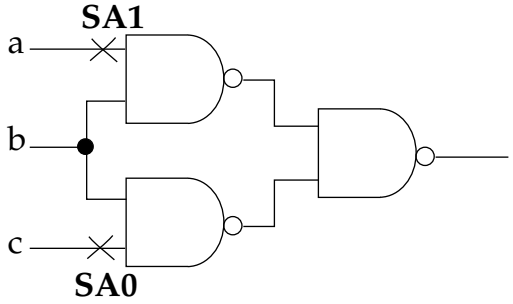
12) (6 pts) Equivalent fault collapsing has been applied to the following circuit and collapsed faults are indicated with an 'X'. Apply dominance fault collapsing and list the faults that remain!



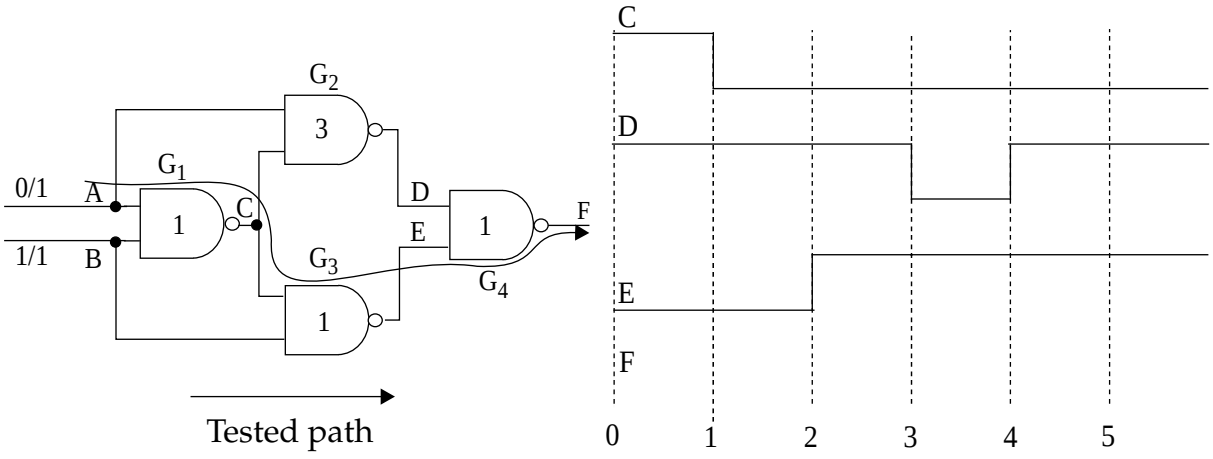
13) (4 pts) Give the test sequence needed to detect all stuck-open faults for the following 2 input NOR gate.



14) (4 pts) The single stuck-at fault model assumes exactly one fault is present in the circuit. Give the test for *C SA0* and show that it is not possible to detect it when *A SA1* is also present in the circuit. What is this called?



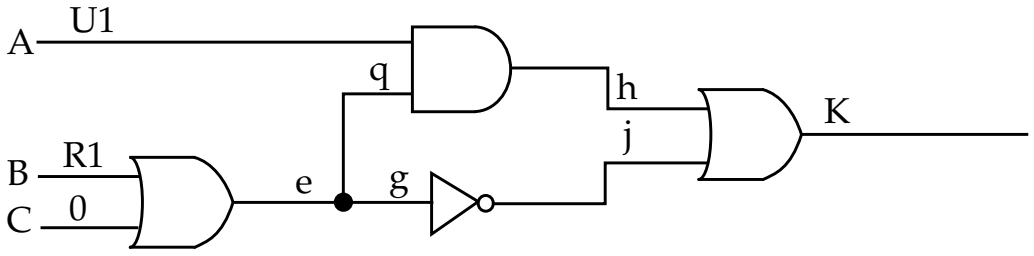
15) (6 pts) Draw the waveform for output *F* given the gate delay assignments and test sequence shown in the figure. What type of hazard is produced?



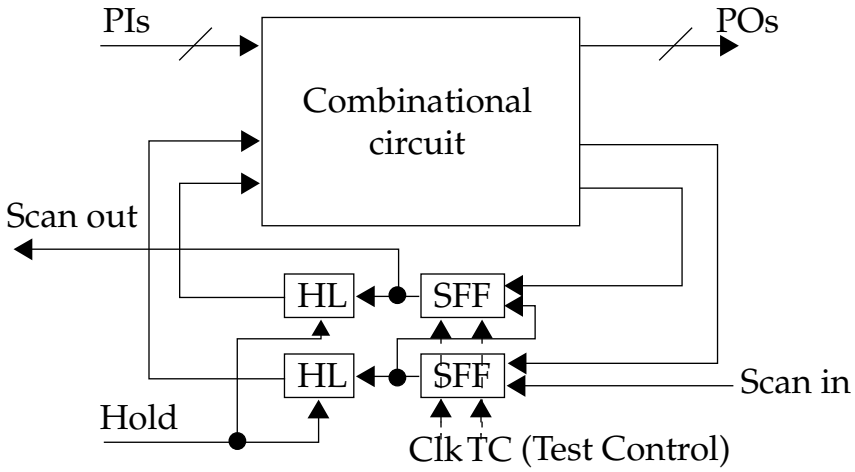
16) (4 pts) Is the test of path *A-C-E-F* in the above circuit *hazard-free robust*, *robust* or *non-robust?*

17) (6 pts) If the on-path input to a gate along a tested path changes from the *dominant* input state to the *non-dominant* input state of the gate, what are the constraints on the behavior of the off-path nodes in order for the test to be robust?

18) (6 pts) Given two paths *P1: B-e-g-j-K* and *P2: B-e-q-h-K*, briefl ydescribe why a rising transition on P2 is a non-robust test. Annotate the diagram with rising and falling waveforms as appropriate.



19) (4 pts) The following scan-path architecture for performing delay test is called *enhanced scan test*. As a circuit designer (not a test person), identify the undesirable characteristics of this architecture.



20) (6 pts) Launch-on-shift and launch-on-capture are two alternative strategies for performing delay test in a scan environment. Briefl yexplain how V_2 is generated in each of these schemes.